

Low Capacitance SWIR Photodetectors for High Speed Sensing Applications

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ABSTRACT

Sensors Unlimited Inc. (SUI), a Collins Aerospace Company, has developed a large-area, high-speed, short-wave infrared (SWIR) focal plane array (FPA) to meet the field-of-view (FOV) and bandwidth requirements of LiDAR applications. Modifications to SUI's standard InGaAs photodiode array (PDA), include junction shape, dielectric thickness, and contact metallization. These changes allow for a reduction in the effective capacitance seen by the hybridized FPA's readout integrated circuit (ROIC) while preserving the epitaxial structure that ensures the company's industry-leading dark current. Compared to SUI's standard device, significant capacitance reductions have been demonstrated. Enhancements of laser pulse detection performance arising from the capacitance improvement, and suitability of the resulting device for implementation in LiDAR systems, will be discussed.

Keywords: PDA (Photodiode Array), low-capacitance, FPA (Focal Plane Array), high-speed photodetectors, LiDAR, LaDAR, InGaAs, SWIR

1. INTRODUCTION

For optical detection systems such as cameras, laser spot tracking, laser coded-pulse tracking, laser-range finders and Light Detection and Ranging (LiDAR) systems, detector arrays made with Indium Gallium Arsenide (InGaAs) are an excellent choice when the system needs to operate at wavelengths longer than 950 nm, where silicon response becomes very weak. In such optical detection systems, electrical amplifiers operating with low noise is essential. The noise of the detector and amplifier combination is an important determining factor in the system sensitivity and hence the ability to detect emitted and reflected light from long distances. The lower the noise of the detector-amplifier combination, then the lower the overall system noise and hence the lower level of light signal that can be detected. The electrical noise of the amplifier is determined partially by the capacitance of the photodiode and its contacts, including any stray capacitances. The larger the total capacitance, the higher the detection noise floor of the amplifier.

Sensors Unlimited Inc. (SUI), a Collins Aerospace Company, is developing high-speed, short-wave infrared (SWIR) focal plane arrays (FPA) to meet the increasing field-of-view (FOV) and bandwidth requirements of laser pulse detection and imaging applications, including for LiDAR. This work will present modifications to SUI's standard InGaAs photodiode array (PDA) designs, including junction shape, dielectric passivation design, and hybridization bump shape and contact metallization. To achieve low capacitance, unique design of the epitaxial structures [1, 2] and of the diffusion process is required. This can involve highly complicated epitaxial growth and photodetector processing steps. The resulting capital and labor expenses could therefore become very high. The photodetector dark current may also be dramatically increased, which in turn results in high system dark noise for both APD and high-speed PIN photodetector designs. In addition, for most APDs there will be high gain, amplifying the front-end noise.

The modifications developed by SUI have been demonstrated to reduce by over 50% the effective capacitance load on the FPA's readout integrated circuit (ROIC) while preserving the company's industry-leading low dark current resulting from its proprietary epitaxial structure design [3].

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The use of high-aspect-ratio bumps (HAR-bumps: height greater than the width of the bump) enables reducing the area of the bump contact metal on both the PDA and ROIC sides. This reduces the capacitance contribution of metal area. The HAR-bumps permit using a wider gap between the PDA and ROIC, reducing potential capacitance coupling of parallel contact metal areas and accommodating bow curvature between the PDA and ROIC for improved uniformity. Proprietary methods for creating HAR-bumps with flat tops reduce can be found from previous SUI work [4]. The corresponding lateral expansion of the bump is also reduced in this case, which furthers reduces the capacitance.

The design improvements can be applied to both high-speed P-I-N photodiode arrays and for detector arrays made as Avalanche Photo Diodes (APD) arrays. In both cases the presented design provides for achieving the best camera performance in applications such as low-light imaging, coded-pulse tracking and for laser range-finding. The modifications can also be applied to bump-bonded 1-D (linear) arrays. Enhancements of laser pulse detection performance arising from the capacitance improvement, and suitability of the resulting device for implementation in LiDAR systems, will be discussed.

2. METHODOLOGY

2.1. Photodiode Array Fabrication

This paper investigated the impact of critical control factors on photo detectors capacitance by targeting low device capacitance. In the meantime the excellent performance and reliability of the photo detectors were maintained to preserve the company's industry-leading low dark current, high uniformity, minimal defects and high operability photo detectors. The fabrication process for low capacitance PDAs is similar to that for SWIR InGaAs PDAs from SUI [5, 6]. In our PDA process, the epitaxial structure for InGaAs *p-i-n* photodiodes consists of an *n*-type indium phosphide (InP) substrate, followed by an intrinsic InGaAs absorption region, and topped off with an InP cap. InGaAs photodiodes can be either front or backside illuminated. Single-element photodiodes and 1-D arrays are mostly front side illuminated, while 2-D arrays are backside illuminated due to the indium-bump-bonding process used to integrate the arrays with a CMOS readout circuit. In the case of backside-illuminated arrays, a "planar/mesa" process was used in which the individual photodiodes are planar with all the processing done through holes in a passivation coatings. The entire photodiode array was isolated on a mesa that allows front-side electrical contact to the common-cathode substrate. The photodiode arrays were then flip-chip bonded to a ROIC. Once the PDA and ROIC have been pressed together, an epoxy was wicked between them. This epoxy held the hybridized device together and provides critical support to the PDA.

Modifications to SUI's standard InGaAs photodiode array (PDA) included designing junction shape by adjusting diffusion depth for multiple epitaxial thickness as well as passivation dielectric thickness. By introducing intervals of Oxide and Nitride layers, the layer thickness and dielectric constant were optimized while still keeping low-coating stress, which normally was resulted from thick coatings. The use of high-aspect-ratio bumps (HAR-bumps: height greater than the width of the bump) reduced the area of the bump contact metal on both the PDA and ROIC sides. The capacitance contribution of the metal areas was therefore reduced. The HAR-bumps allowed using a wider gap between the PDA and ROIC, which reduced the potential capacitance coupling of parallel contact metal areas and accommodated the bow curvature between the PDA and ROIC for improved uniformity. Proprietary methods for creating HAR-bumps with flat tops could be found from previous SUI work [4]. The corresponding lateral expansion of the bump was also reduced in this case, which resulted in further reduction of the effective capacitance. Compared to SUI's standard device, significant capacitance reductions have been demonstrated in this work.

2.2. Characterization

Characterization of the photodiode diffusion, etch, passivation, metallization and other critical process steps was performed using High Resolution Scanning Electron Microscope [Hitachi] for morphology; Electron Dispersive Spectrometry [Bruker] for material content; surface optical profilometry [Wyko] for surface morphology and roughness; Zygo Profilometer for bowing and stress and optical microscopy [Olympus] and surface profilometry [KLA] for step height, etch rate and profile. Current-voltage (I-V) measurements were carried out to compare multiple Design of Experiment (DOE) case dark current and Process of Record (POR). Capacitance-voltage (C-V) measurements for diodes, MIS and shorted pixels capacitance scan were also performed.

3. RESULTS AND DISCUSSION

3.1. Device Structure and key Contributors for Capacitance Improvement

Figure 1 presented the PDA cross section. Epitaxial structure for InGaAs *p-i-n* photodiodes included an *n*-type indium phosphide (InP) substrate, followed by an intrinsic InGaAs absorption region, and topped off with an InP cap. InGaAs photodiodes were backside illuminated because of the indium-bump-bonding process used to integrate the arrays with a CMOS readout circuit. Individual photodiodes were planar with all the processing done through diffusion holes in passivation coatings. The entire photodiode array was isolated on a mesa that allowed front side electrical contact to the common-cathode substrate. Key capacitance contributors included designing junction profile by adjusting diffusion depth and lateral diffusion for various epitaxial cap, absorption layer doping and thickness combinations, passivation dielectric thickness and stack layers dielectrics constant, as well as contact metal stack material combination, aspect ratio and foot print.

The key contributors for device capacitance will be discussed here as illustrated in Fig 1 and Table 1.

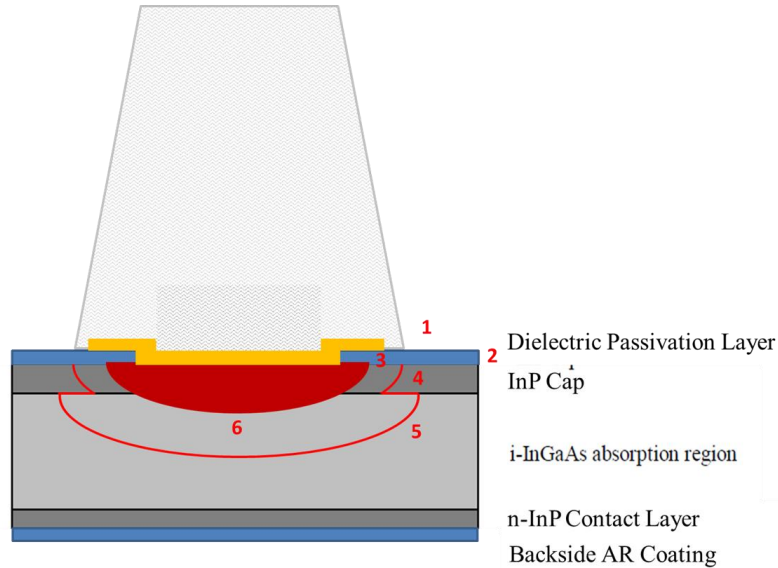


Figure 1. Cross section of the photo diode array with key contributors numbered

Table 1. Key Contributors and their effect on device interconnection capacitance

Factor	Contributors	Capacitance Effect
1	Contact Metal Foot Print	Larger foot print will increase the contact diameter, capacitance will increase
2	Dielectric Stack	Both dielectric constant and layer thickness will affect the capacitance by affect the distance, dielectric constant and stress
3	Diffusion, Doping	Lateral and vertical diffusion profile and doping concentration will affect depletion width and depth
4	Cap, Doping	Depletion profile, concentration
5	Active Layer , Doping	Depletion profile, concentration
6	Diffusion Depth	Diffusion into the active layer, depletion profile

3.2. Device Simulations

Two-dimensional simulations have been carried out to investigate process parameters affecting device capacitance. Figure 2 (a) represents a single photodiode pixel with interconnect metallization (shown in yellow), while Fig. 2(b) includes the additional metal associated with the mating ROIC indium bump. The increased metal thickness did not affect the capacitance.

Simulations of five adjacent pixels are shown in Figure 3(a) and 3(b), where the passivation thicknesses was varied. By increasing the passivation thickness, the normalized capacitance was reduced by approximately 25% as shown in Fig. 3 (c) and (d). The reduction is attributed to the increased distance between the overhanging metal of the interconnection and the semiconductor beneath.

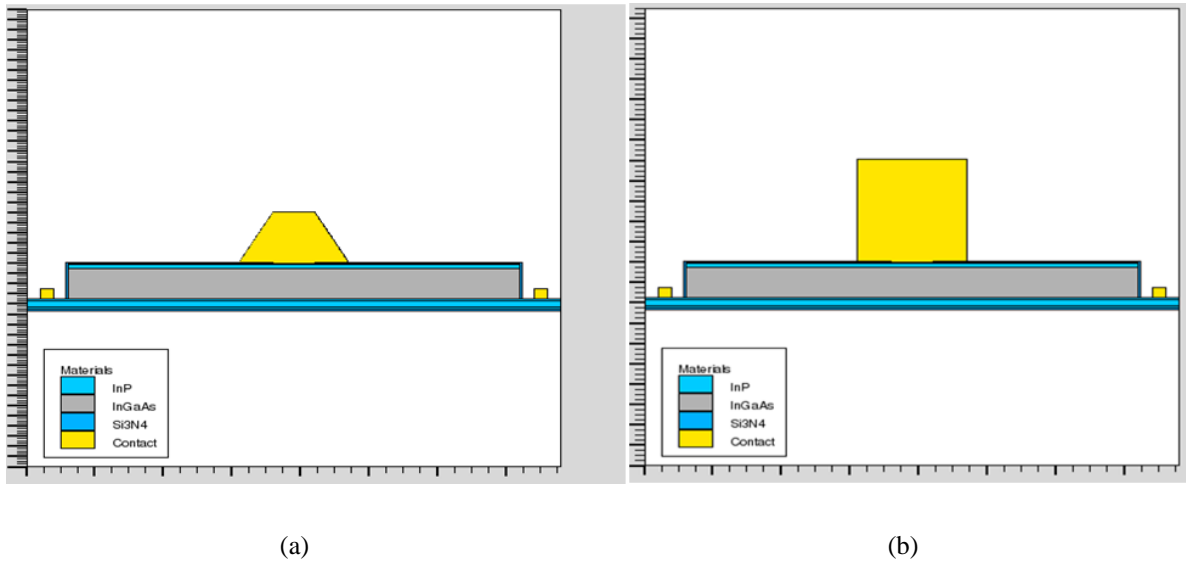
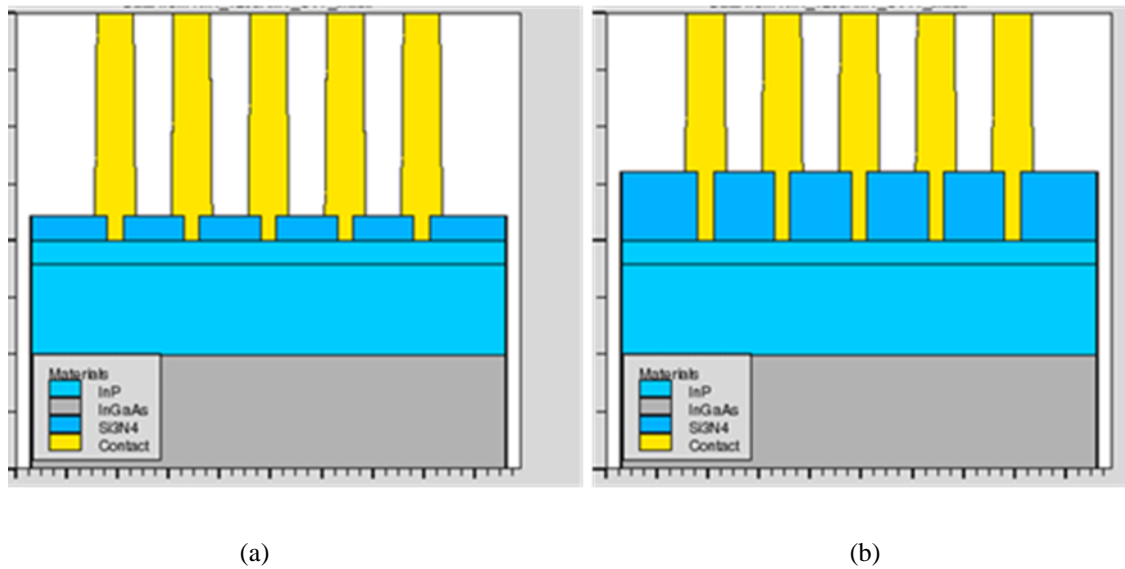


Figure 2. Simulation for single pixel case with (a) PDA metal contact and (b) both PDA and ROIC metal contact



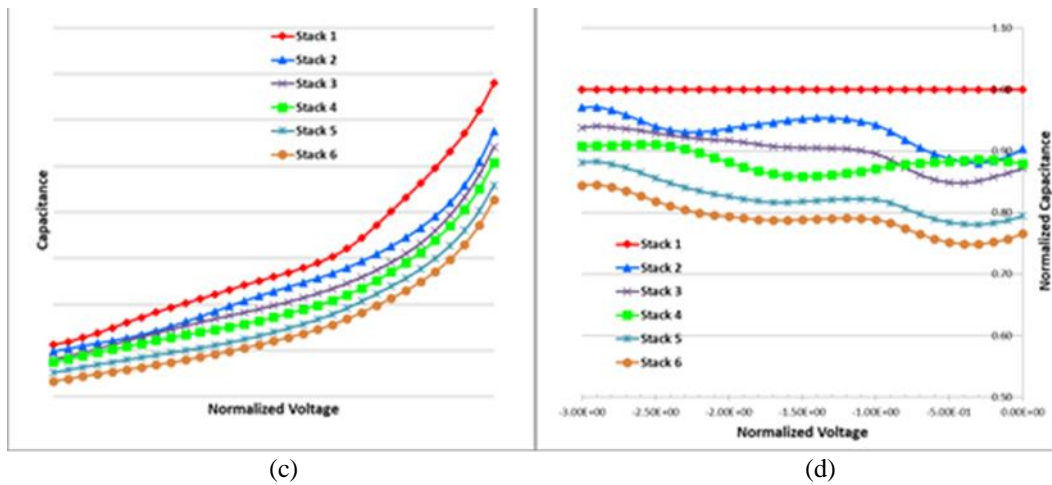


Figure 3. Multi-pixel simulation results on effect of dielectric thickness on capacitance. (a) Standard case, (b) DOE stack with different passivation thickness (c) Normalized C-V curve for different dielectric stacks (d) Comparison of normalized capacitance over normalized bias for different dielectric layers.

3.3. Junction Shape Effect on Dark Current and Capacitance

As discussed in section 3.1, epitaxial structure in combination with diffusion profile played a key role on defining depletion depth and width. All of these will affect the optimization of both dark current and device capacitance. In this work, multiple combinations of cap thickness, absorption layer thickness, doping and diffusion profiles have been investigated. Epitaxy structure and diffusion depth as well lateral diffusion have been measured from SEM top view and cross section as shown in Figure 4. Design of Experiment (DOE) conditions of key control parameters on epitaxy and diffusion have been listed in Table 2, which contains normalized data relative to a wafer made to the standard SUI recipe.

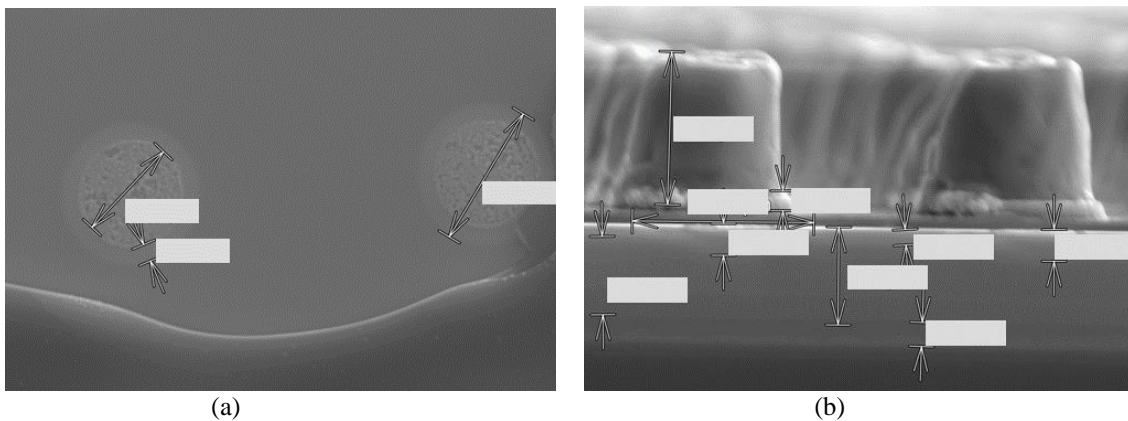


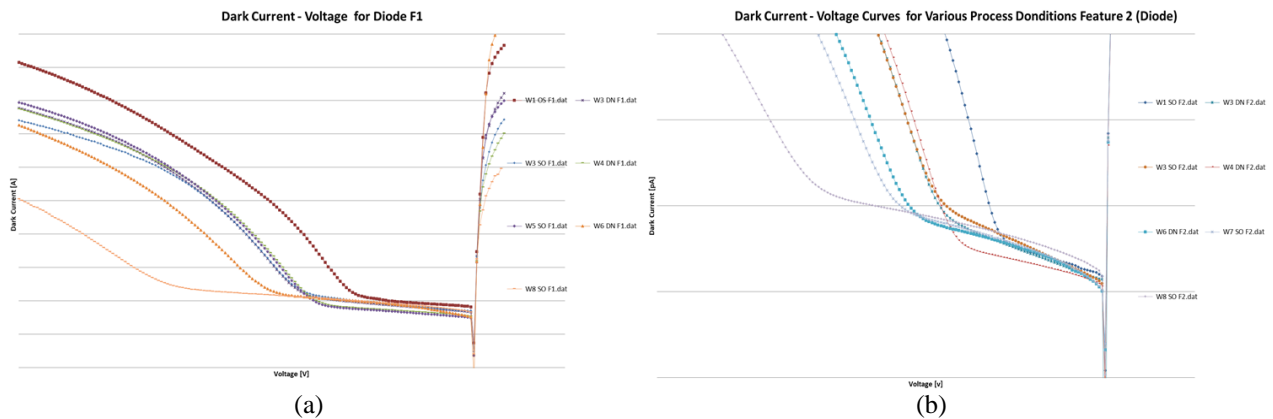
Figure 4. SEM (a) Top view and (b) Cross Section for epitaxy structure and diffusion profile

Table 2. DOE Matrix for Epitaxy and Diffusion Profiles

Wafer Id	Norm Cap Layer	Norm Absorption Layer	Norm Diffusion Depth	Norm Lateral Diffusion
1	0.5	0.8	0.6	0.6
2	1.0	1.0	1.2	1.0
3	0.7	1.0	0.9	0.8
4	0.7	1.0	0.9	0.8
5	0.7	1.0	0.9	0.8
6	1.0	1.0	1.2	1.1
7	1.0	1.0	1.2	1.1
8	2.0	1.2	2.0	2.0

3.3.1. Junction Shape on Dark Current

Figure 5 compared multiple combinations of cap layer thickness, absorption layer thickness and diffusion profiles on dark current. By comparing both the full IV behavior from multiple diode features, dark current has been optimized from the combination of normalized cap and absorption as shown in Fig. 5 (a)-(c). When considering the effect of epitaxy layer and diffusion layer thickness on dark current, on the one hand, reduced layer thickness will decrease the lateral and vertical diffusion for thinner cap, which will lower the dark current due to the reduced diffusion surface area. On the other hand, thinner epitaxy layers may come with more interface defects from epitaxial growth for sudden layer content change. This will increase the device dark current due to the increased leaky path resulted from the interface defects. Good linearity was achieved between lateral width and vertical diffusion depth as shown in Fig. 5 (e). Similar trend for dark current density has been obtained on pixel array dark current which shorted certain amount of pixels together for measurement as shown in Fig. 5 (f). Dark current density for pixels has been optimized here similarly as discussed for diode ones in Fig. 5 (a)-(c). To understand the effect of diode feature on dark current, multiple diode dark current densities have been compared as shown in Fig. 5 (g) for different areas and perimeter over Area (P/A). Dark current density reduced with pixel area while increased with P/A, which means more leaky paths at diffusion and dielectric opening interface.



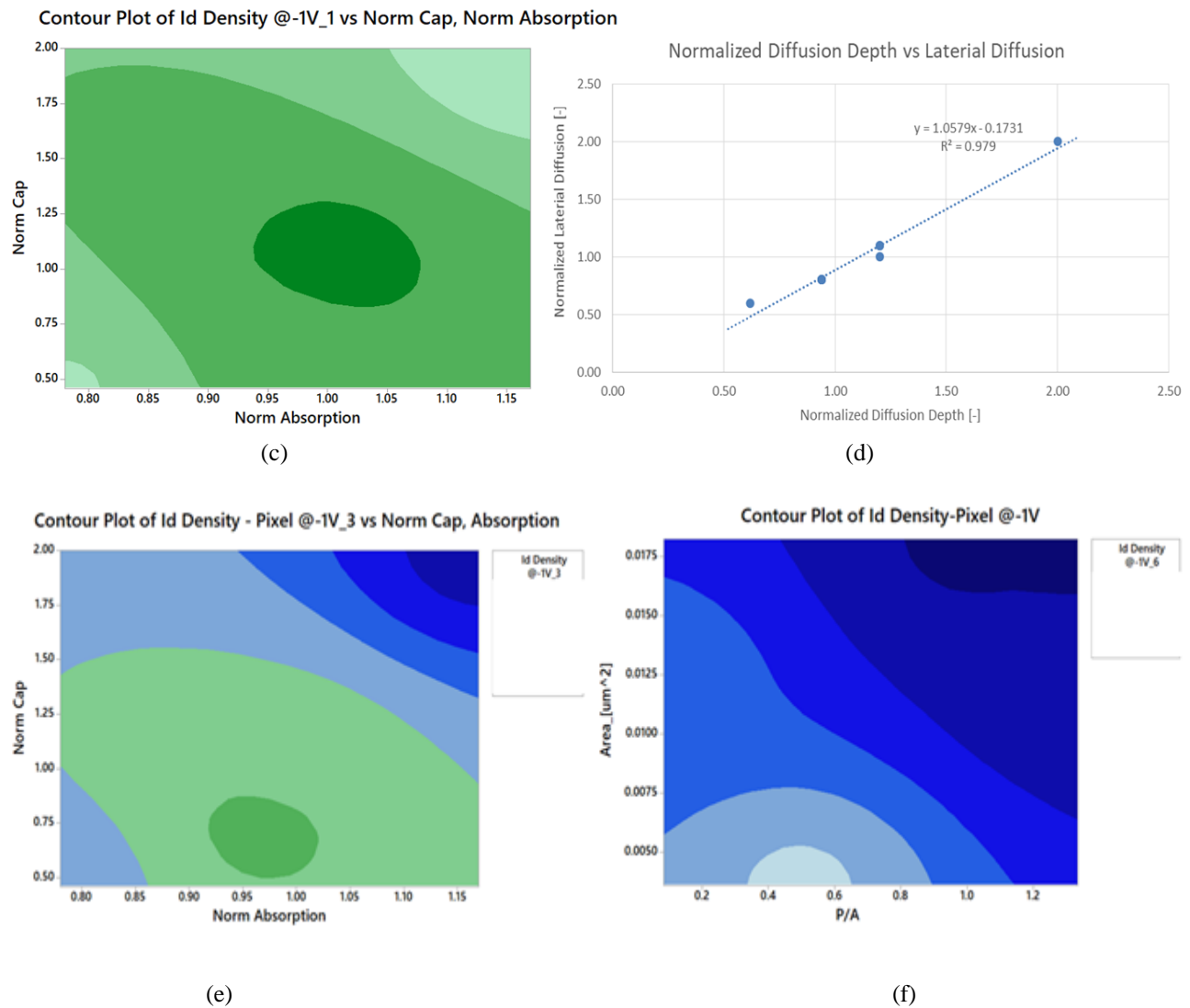
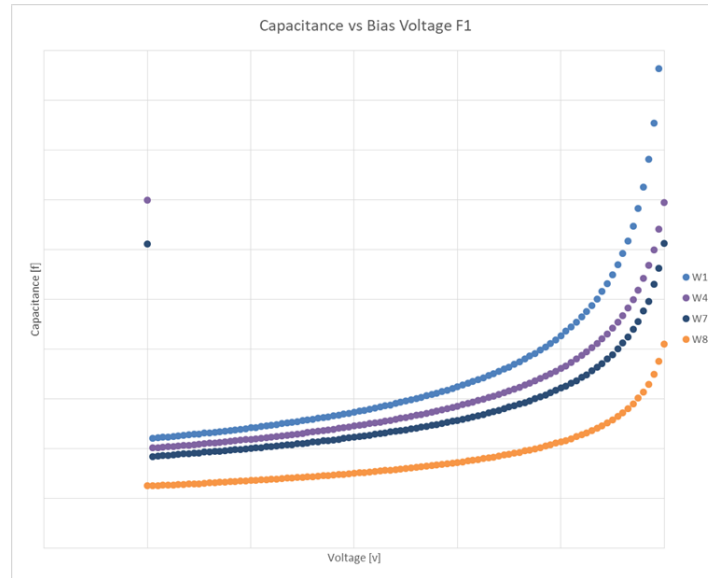


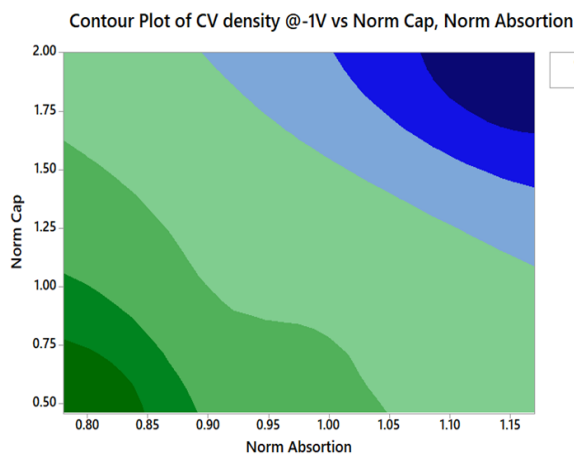
Figure 5 (a) Diode and Pixel Dark Current, (b) Current –Voltage curve for test diodes, (c) Contour plot for diode dark current density vs normalized cap and absorption layer (d) Comparison of normalized lateral vs vertical diffusion (e) Contour plot for pixel dark current density vs normalized cap and absorption layer, and (f) Contour plot for dark current density vs area and P/A.

3.3.2. Junction Shape on Capacitance

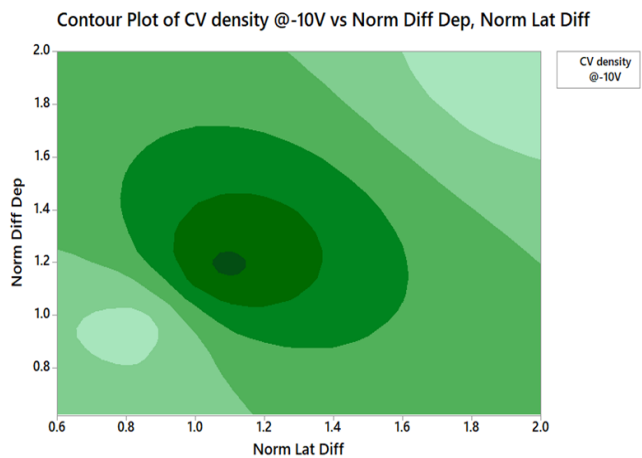
Capacitance and Voltage (C-V) of the same diode feature from various epitaxial structured wafers have been tested and compared in Figures 6 (a)-(c). Different combinations of cap, absorption, diffusion depth and lateral diffusion have been investigated. Optimized capacitance has been obtained from normalized cap and absorption combinations. Diffusion profile changed with different cap and absorption layers so that vertical and lateral diffusion changed accordingly. As a result, the junction depletion width and area increased or decreased together. The balance of this competition of depletion width and area determined the device capacitance.



(a)



(b)



(c)

Figure 6 (a) Capacitance vs Voltage (C-V) of the same diode feature from various wafers, (b) CV density contour map for different combinations of cap and absorption, and (c) CV density contour map for diffusion depth and lateral diffusion

3.4. Dielectrics Stacks Discussion

Well controlled stress is essential for device processing which eventually will affect photo, bowing and hybridization of PDA to ROIC. Too much stress may also jeopardize the integration of dielectric passivation, in which case, the electrical performance will be affected. In this work, diode surface passivation in the bump contact area has been created by interleaving layers of Oxide and Nitride layers. This reduced the capacitance contributed by the passivation through increasing the dielectric constant and layer thickness. The interaction of the two dielectric layers reduced the stress that would normally be experienced with thick passivation.

Figures 7 (a) and (b) compared electrical behavior from different combinations of metal and dielectrics stacks. Various metal stacks have been applied to the same wafer. As presented in Fig. 7(a), there was no change for dark current density for diodes with different shapes, which has been validated from different features (P/A). Fig. 7(b) compared I-V behaviors side by side for different dielectric stacks comparison, i.e. POR vs DOE. There was no dark current change for different dielectric stacks through the whole bias range, which has been verified from different features.

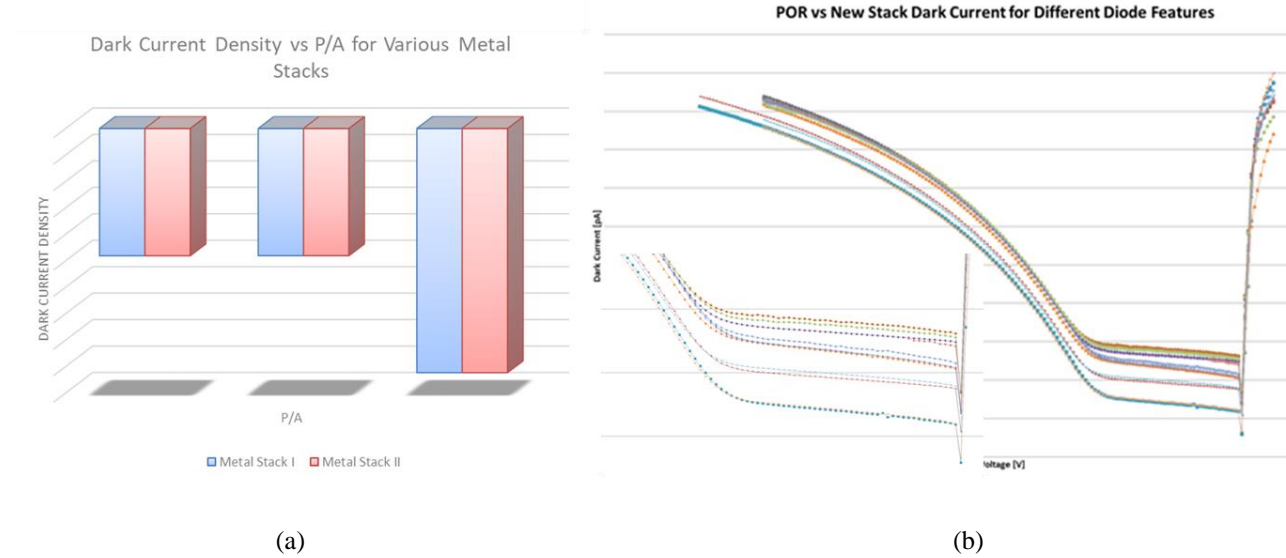


Figure 7 (a) Dark current density for various metal stacks out of the same wafer (b) IV behavior comparison for POR and DOE stacks of different diode features

3.5. Pixel Capacitance

3.5.1. Extraction of Pixel Capacitance

For pixel capacitance, a test structure as shown in Figure 8 has been designed for measuring the detector capacitance. The quantities for calculating the capacitance of one detector were listed in Table 3. For the A structure, the total number of diodes is the same while the contact metal area has been changed. For the B test structures, the number of detectors varies while the total area of the contact metal is the same. Since the detector capacitance includes the contact metal, for each detector that is added the corresponding area of metal needs to be subtracted,

$$\begin{aligned}
 C_{\text{total}} &= nC_{\text{detector}} + (A_{\text{totalmetal}} - nA_{\text{detectormetal}})C_{\text{per area for metal}} \\
 &= n(C_{\text{detector}} - A_{\text{detectormetal}}C_{\text{per area for metal}}) + A_{\text{totalmetal}}C_{\text{per area for metal}} \\
 &= na + b
 \end{aligned}$$

Here, it was assumed that any capacitance due to fringing fields or between the detectors was negligible. A line fit to the data could be used to calculate the capacitance per detector pixel,

$$\begin{aligned}
 C_{\text{detector}} &= a - A_{\text{detectormetal}}C_{\text{per area for metal}} \\
 &= a - bA_{\text{detectormetal}} / A_{\text{totalmetal}}
 \end{aligned}$$

Example fits were shown in Figure 9. Very good linearity between capacitance versus pixel number as well as capacitance versus contact metal area have been obtained. The calculated pixel capacitance between DOE and POR dielectric stacks were compared in Table 4. A 25-35% improvement of the calculated pixel capacitance for DOE cases has been achieved over varies bias voltages.

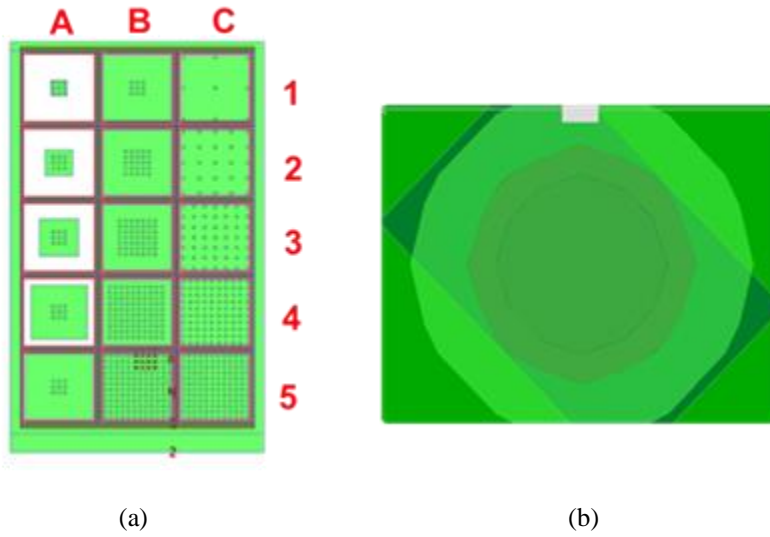


Figure 8. Pixel capacitance test structure (a) Array, and (b) Pixel with diode and contact metal

Table 3. Key parameters for capacitance calculation

Quantity	Units	Comment
Capacitance of one detector	fF	Including both the diode and the overlay metal
Capacitance of the entire test structure	fF	
Total area of the overlay metal in the test structure	μm^2	Area for B structures
Area of overlay metal for one detector	μm^2	Calculated Area
Capacitance per unit area of the overlay metal	$\text{fF}/\mu\text{m}^2$	
Number of detectors in the test structure		Varies for B structures

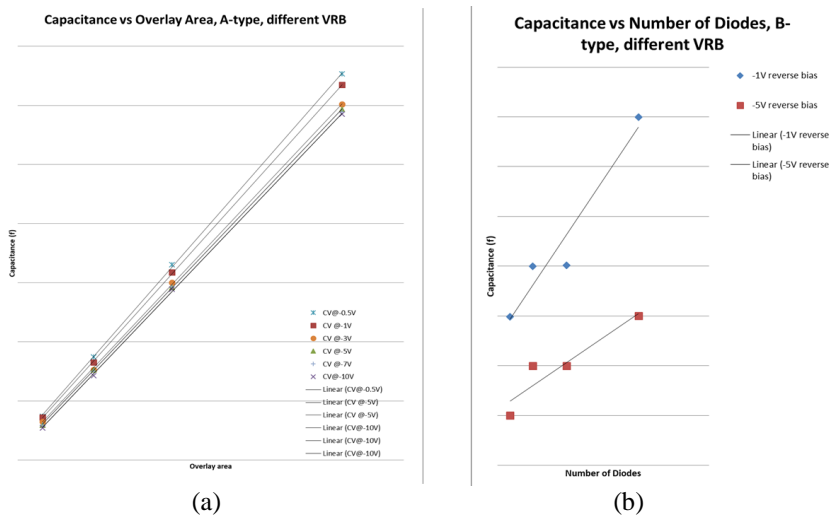


Figure 9. Pixel capacitance values using measured results from (a) Test structure A and (b) Test structure B

Table 4. Comparison of calculated capacitance between DOE and POR dielectric stacks

V_RB	% CAPACITANCE IMPROVEMENT
0.5	28.2
1	34.2
3	34.2
5	25.2
7	21.2
10	26.4

3.5.2. Discussion on Pixel Capacitance

Figure 10 compared different combinations of diffusion and contact metal areas capacitance. For the same diffusion area, if the contact metal area is smaller or the same as the diffusion one, the capacitances are the same. Once the contact metal area is larger than the diffusion one, which is mostly the case for photo diode applications, the capacitance will increase accordingly. Improvement for diode capacitance has been obtained for DOE passivation stack when comparing with the POR one as shown in Fig. 10 (a) by 25-30%. The repeatability is pretty good as shown in Fig. 10 (b).

The enlarged diodes from real pixels with the same metal contact area over diffusion ratio has been tested and compared as shown in Figure 11. Stable CV behavior has been achieved with good repeatability. By comparison of POR and DOE conditions, 50% improvement was achieved for CV reduction by introducing different dielectric stacks.

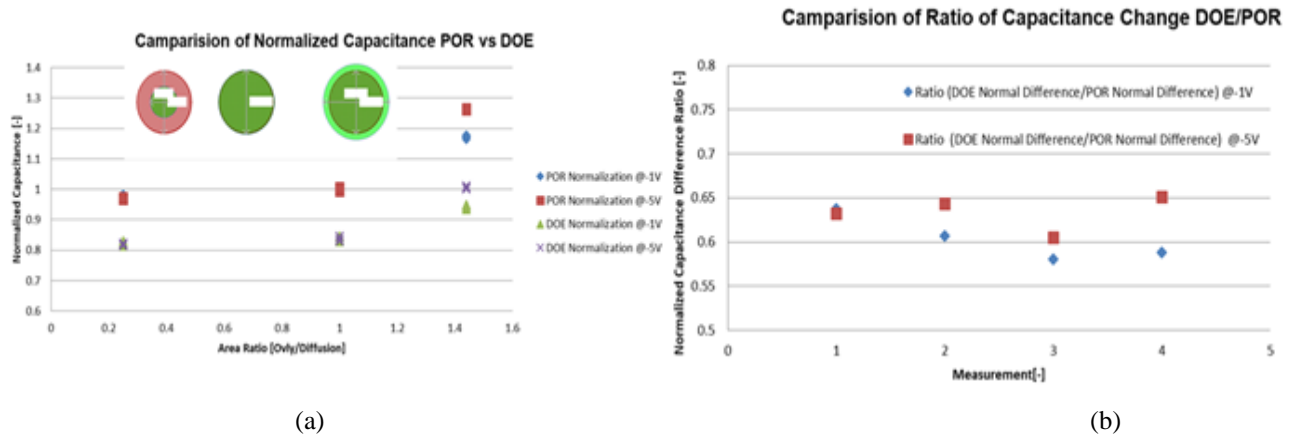


Figure 10. Comparison for various area ratio of diffusion and metal (a) Normalized capacitance for POR vs DOE (b) Repeatability

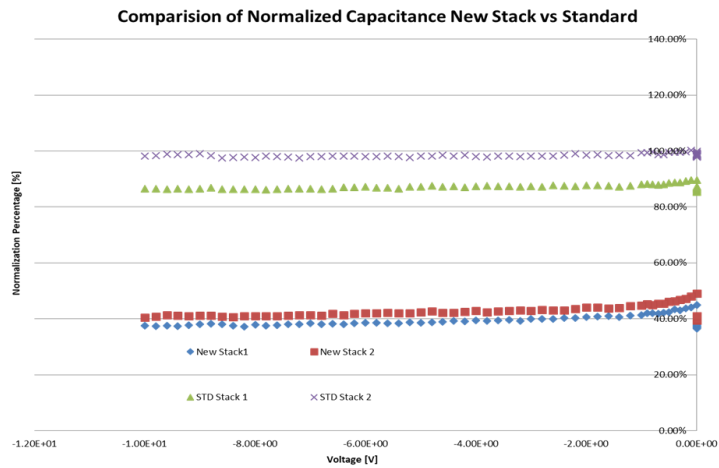
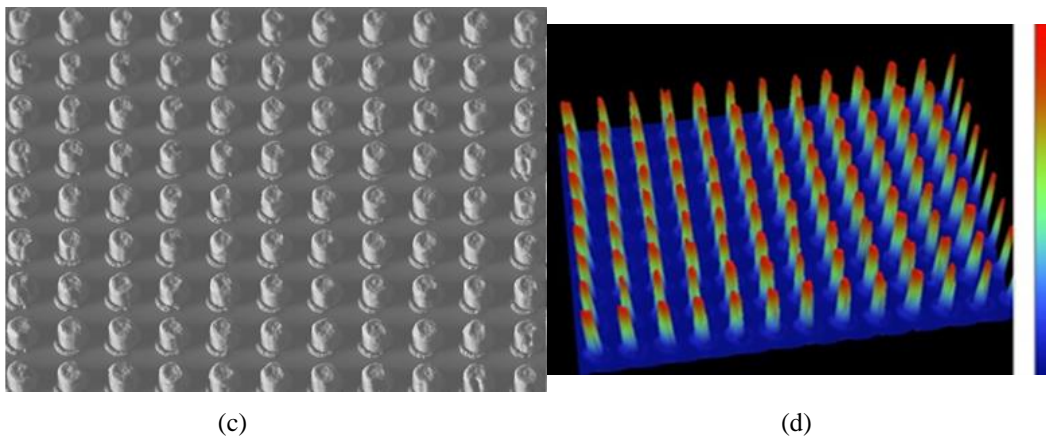
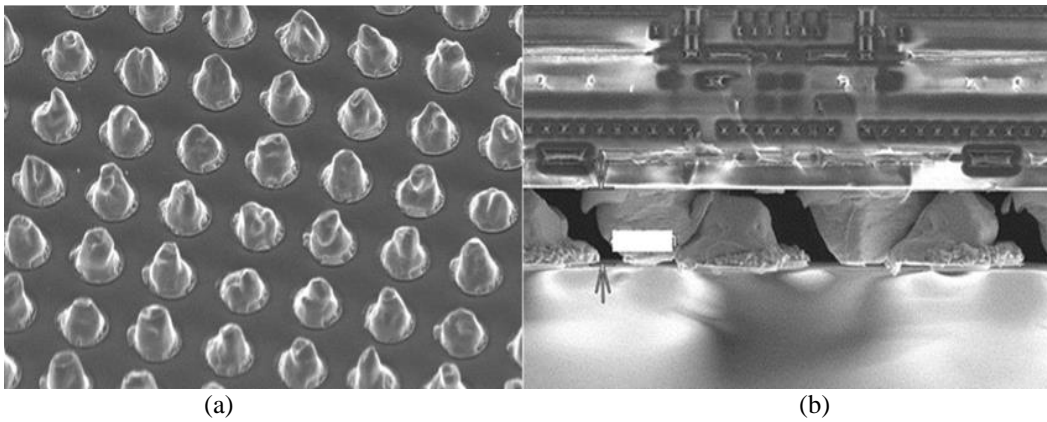


Figure 11. Comparison of normalized capacitance for new stack vs standard

3.6 Effect of Metallization Stack and Hybridization

As discussed in section 3.1, the metal footprint affects the device capacitance, so reduction of metal overhang presents an avenue toward improved device performance. Meanwhile, as discussed in previous work [7-9], non-uniform bumps are a challenge for hybridization, causing misalignment and slippage during pressing which in turn tend to increase the metal footprint, as shown in Figure 12 (a) and (b). Shorting between neighboring pixels can also occur, especially for larger format FPAs with finer pitches. Highly uniform bumps with flat heads have recently been developed [4, 10]. Bump aspect ratios (height:width) above 2:1 were achieved, compared with a traditional ratio of 1:1, over large format die in this work, which enabled reduction of the area of the bump contact metal on both the PDA and ROIC sides, as shown in Fig. 12 (c)-(f). This reduced the capacitance contribution of the contact metallization. The higher aspect ratio allows a wider gap between the PDA and ROIC, resulting in the reduction of the potential capacitance coupling of parallel contact metal areas and accommodating bow curvature between the PDA and ROIC for improved uniformity.



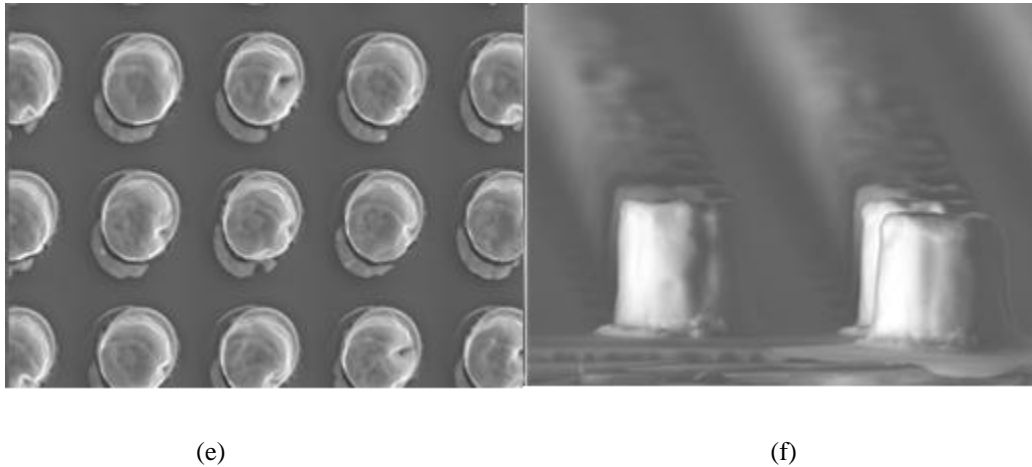


Figure 12 Bumps and hybridization from various processes. Example of non-uniform bumps (a) prior to hybridization (b) in cross section following hybridization. Newly developed bumps: (c) angled SEM of bump array, (d) profilometry, (e) top view SEM and (f) side view SEM.

3.7 Sensor Performance with Effective Detector Capacitance

As mentioned above, the impetus to investigate techniques for reducing the effective capacitance of the detector stems from the desire to improve the sensor performance for active imaging applications, of course, without detrimentally affecting any passive imaging performance. The effective capacitance of the detector as seen by the readout integrated circuit (ROIC) is composed of not only the diffusion capacitance of the photodetector, but also the electrode and any parasitic capacitances associated with hybridization. The sensor's performance dependence on this effective detector capacitance will also be contingent on the ROIC pixel architecture (i.e. direct injection, buffered direct injection, CTIA, etc.) and its design or implementation. Towards this end, SUI simulated the consequence of both increasing and decreasing the effective detector capacitance by $\pm 20\%$. These simulation results are displayed in Figure 13. The results show the output of one of the amplifiers in the analog signal path of one of SUI's pixel designs as a function of the effective input capacitance as seen by this pixel. By decreasing this capacitance by 20%, SUI expects to see a resultant increase in pulse sensitivity [red in (a), purple in (b)] without any unfavorable effect on any other sensor performance parameter.

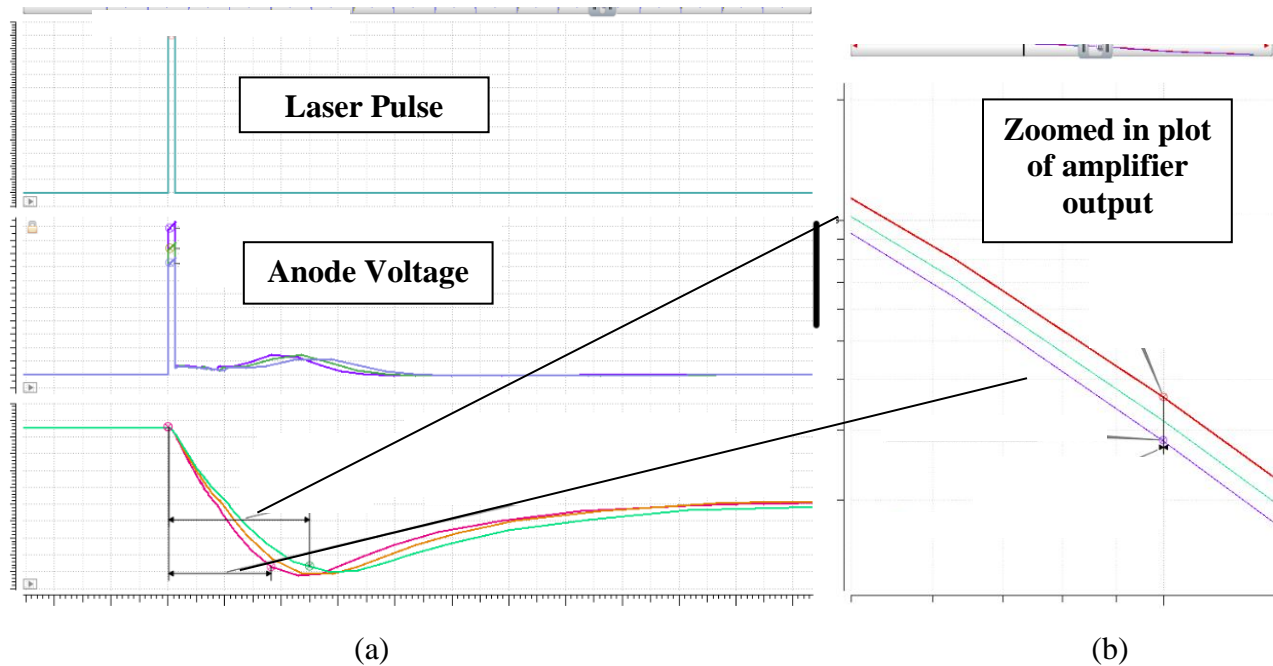


Figure 13 Simulated transient results of one of SUI's ROIC pixel designs showing the effect of increasing and decreasing the capacitance as seen by the pixel input by $\pm 20\%$ for in laser pulse stimulus. The results clearly show an improvement in sensitivity for decreasing input capacitance. a) Transient simulation of laser pulse input and the resultant voltage at the detector anode and amplifier output b) zoomed-in plot of the transient response of the amplifier output; the blue trace shows the decreased capacitance case, while the green and red graphs show the nominal and increased capacitance results, respectively. For (a), red corresponds to the decreased capacitance case, orange corresponds to the nominal capacitance case, and, finally, green corresponds to the increased capacitance case; the graph color coding in (a) doesn't align to the color coding in (b).

4. SUMMARY

Sensors Unlimited Inc. (SUI), a Collins Aerospace Company, has developed high-speed, short-wave infrared (SWIR) focal plane arrays (FPA) to meet the increasing field-of-view (FOV) and bandwidth requirements for simultaneous laser pulse detection and imaging applications such as LiDAR. Modifications to SUI's standard InGaAs photodiode array (PDA) designs, including junction shape, dielectric passivation design, and hybridization bump shape and contact metallization were performed to achieve total effective capacitance reduction. These modifications have been demonstrated to reduce by over 50% the effective capacitance load at the detector and readout integrated circuit (ROIC) while preserving the company's industry-leading low dark current resulting from its proprietary epitaxial structure design. The design improvements can be applied to both high-speed P-I-N photodiode arrays and Avalanche Photo Diodes (APD) arrays. In both cases the presented design provides for achieving the best camera performance in applications such as low-light imaging, coded-pulse tracking and laser range-finding. The modifications presented here can also be applied to bump-bonded 1-D (linear) arrays.

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