

Advanced SWIR APDs for Multimode Applications

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ABSTRACT

Recent short-wave infrared (SWIR) sensors have demonstrated in-pixel multimode capabilities. One of the additional modes is range finding. High resolution range finding is increasingly becoming vital functionality in high precision targeting and imaging systems. Highly precise and accurate range-to-target information is essential for many modern commercial and military applications. With the recent advances in LiDAR (Light Detection and Ranging) technology, range measurement accuracies as low as a centimeter at kilometer ranges. Sensors Unlimited Inc. (SUI), a Raytheon Technologies (RTX) Company, has been developing these multimode sensors using traditional PIN-based InGaAs detector technology. However, the capability of these sensors has been extended through the introduction of Avalanche Photodetector (APD) InGaAs sensors. This APD technology has been developed onshore to better serve the onshore community requiring simultaneous laser tracking, ranging, and imaging applications.

In this work, SUI offers an update on previously presented, PDA-specific development, most specifically related to the advancement of Geiger Mode Avalanche Photodetectors (GMAPD). SUI's APD technology is in direct response to the challenging SWaP and NEI performance requirements of active imaging and tracking applications. This update includes 2D and 3D TCAD simulation results with a comparison with measured performance results. Finally, initial results related to the advanced development of Geiger Mode Avalanche Photodetectors (GMAPD) themselves as well as supporting electronics is given. The revitalization of SUI's APD development is a direct response to the challenging SWaP and longer-range with higher accuracy performance requirements of active imaging applications. SUI's most recent APD design improvements facilitates greater signal to noise ratio at the pixel, which subsequently enables a supporting ROIC pixel design with improved performance.

Keywords: GMAPD, LMAPD, APD, LiDAR, LADAR, InGaAs, SWIR, FPA

1. INTRODUCTION

InP/InGaAs avalanche photodetectors (APDs) have been widely used in fiber optic communication systems, 3D LiDAR imaging, free space optical communications, and other systems. With the advances in epitaxial growth of compound semiconductors using Metal Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) methods, there is an increasing interest in large format APDs in the shortwave infrared (SWIR) wavelength range.

In this article, we present a planar InP/InGaAs avalanche photodetector structure designed to manufacture large format focal plane arrays (FPAs) using matured fabrication technologies. The design consists of planar InP/InGaAs avalanche photodetector structure employing n-InP multiplication layer for relatively easy fabrication with no guard ring. Other device structures such as super lattice, staircase, multi-quantum well and I²E device structures has been considered to reduce excess noise factor and increase the gain-bandwidth product [1, 2, 3], but their practical use has also been limited due to difficulties associated with the fabrication processes.

In this work, we demonstrate the design, simulation, epitaxial growth, fabrication and characterization of large format InP/InGaAs separate absorption, grading, charge and multiplication (SAGCM) layer APD arrays with fine pixel pitch (e.g. < 25 μm) operating in Geiger Mode (GM). Our previously presented work displayed mainly the experimental results of the InP/InGaAs avalanche photodiodes [6] operating in the linear mode. In this paper we present simulation results as well as experimental results of the InP/InGaAs avalanche photodetector structure operating both in linear mode as well as Geiger mode (above breakdown voltage).

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2. DEVICE DESIGN

In Avalanche Photodiodes (APDs), that are biased slightly below the breakdown voltage, photogenerated carriers undergo an impact ionization process, generating avalanche multiplication and a finite gain [7]. APDs that operate in linear/analog mode exhibit maximum useful gain that is limited by strong fluctuations during the multiplication procedure. Thus, APDs operating in this regime are unsuitable for time correlated imaging techniques, where single photon sensitivity and an effective time-gating of the detector are typically required. Instead, APDs can be designed and operated above the breakdown voltage, which is called the Geiger mode of operation [8].

During Geiger mode operation, when a photon is absorbed in the multiplication region of the APD, a self-sustaining avalanche is triggered and the current increases rapidly to a well-detectable level in only picoseconds after the photon was absorbed. An external circuit is then needed to quench the multiplication process and restore the APD to its original state, preparing it to detect another photon [9]. The main drawback of APDs with respect to linear mode/analog detectors is the presence of a deadtime after each photon detection which limits the maximum count rate. To bring together the advantages of single-photon detection, typical of GMAPDs, and the photon number resolution, typical of analog detectors, solid-state photodetectors made of GMAPDs operated below breakdown and above breakdown voltage are widely exploited. In addition, the possibility to count each triggered avalanche is achievable both in an analog fashion, where each pixel employs multiple fast resets, integrating every pixel with its own active or passive quenching and amplification/digitization circuitry.

Figure 1 shows such a planar detector structure designed using InP/InGaAs material system to operate in SWIR wavelength region of 1000 to 1700nm. In this device structure, the multiplication region consists of undoped InP layer coupled with charge control layer composed of n type region. These coupled layers provide a high and uniform electric field in the multiplication region. The separated electric field in the multiplication and absorption layers can effectively reduce the band-to-band tunneling and enables the operation of avalanche photodiode at higher gain voltages [4, 5]. This high electric field causes increase in the impact ionization collision rate of both electrons and holes. High electric field in the multiplication region reduces the carrier path length, transit time and avalanche buildup time. The thickness and carrier concentration of the InP charge control layer is optimized keeping the total charge density to be constant for high performance. InGaAsP graded layers mitigate the hole trapping effects due to the abrupt heterojunction band offset between the InP and InGaAs absorption layers. The absorption layer thickness can be optimized to balance the quantum efficiency and the timing response in analog mode. In linear mode, by optimizing the device structure, a gain bandwidth (GBW) product as high as 200 can be achieved with this device structure [6]. To achieve a high gain bandwidth product, a thin multiplication layer width is essential to reduce the avalanche build up time [10, 11]. A thin multiplication layer also has other secondary effects such as enhanced ionization coefficients ratio on high-speed operation of avalanche photodetector [12]. Therefore, one must carefully control the diffusion depth to maintain the thinness of multiplication region.

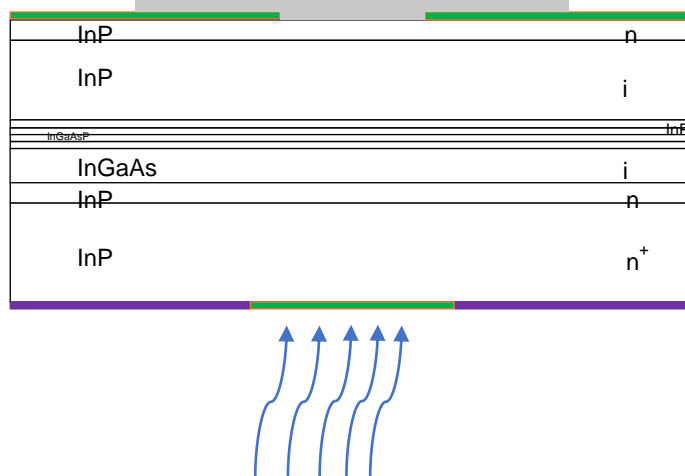


Figure 1. Schematic cross-section of back-illuminated InP/InGaAs avalanche photodiode.

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3. DEVICE SIMULATIONS

Figure 2 shows the two-dimensional (2D) and three-dimensional (3D) device cross-section of the simulated back illuminated planer InP/InGaAs avalanche photodiode. Multiple pixels with a pitch as small as 5 μm were simulated simultaneously to estimate the electro-optical cross talk between the pixels at the dedicated operating bias voltage. In the GMAPD arrays, one of the key performance parameters is the optical crosstalk whereby the avalanche operation in one pixel creates a detectable electrical carrier in the neighboring pixels. One technique to reduce the optical crosstalk is to fabricate the pixels with isolation trenches. Both the planar devices without trenches between the pixels and with etched isolation trenches were simulated to understand the crosstalk behavior and hence the detector-level Modulation Transfer Function (MTF) performance. Figure 3 shows the Scanning Electron Microscope (SEM) cross-section of one of the fabricated InP/InGaAs avalanche photodiode device structures. One of the important fabrication process requirements of the planer InP/InGaAsP based avalanche photodiodes is the ability to precisely control the diffusion depth in the avalanche region. The position of the junction in the avalanche region defines the punch-through voltage, the breakdown voltage, and the amount of gain at the dedicated operating voltage.

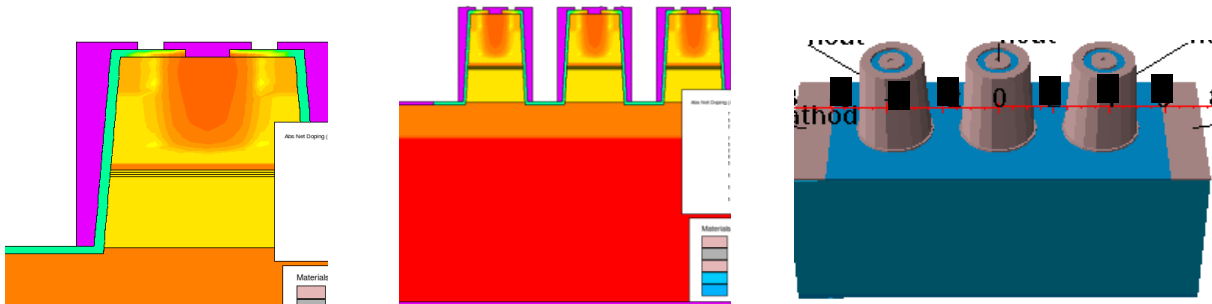


Figure 2. 2D and 3D simulation cross-section of back-illuminated InP/InGaAs avalanche photodiode.

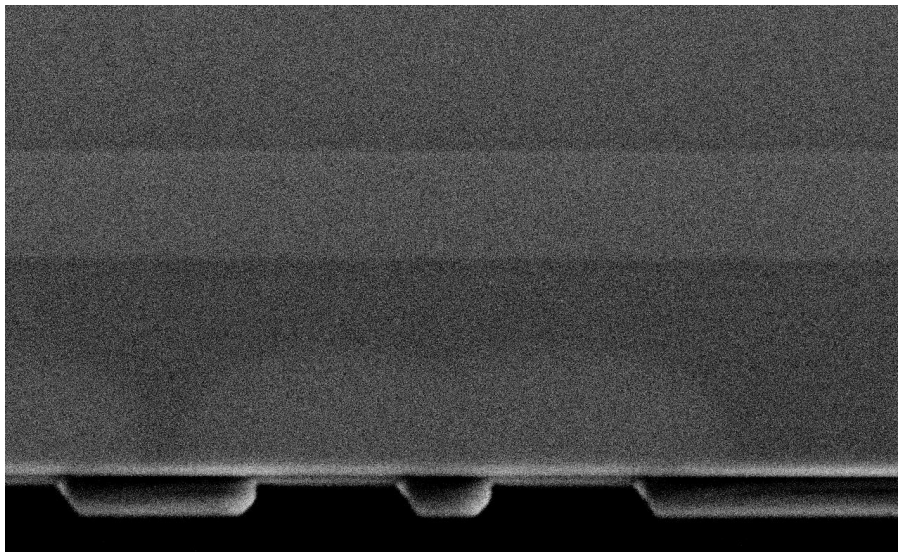


Figure 3. SEM cross section of a fabricated back-illuminated InP/InGaAs avalanche photodiode. One can clearly identify the diffusion, the charge control, and the absorption regions.

Figure 4 shows the simulated gain as a function of reverse bias voltage of the planer InP/InGaAsP based avalanche photodiode. As seen from this figure, a moderate gain (e.g. > 20) is achievable with this device structure. Also, shown in Figure 4 is the variation of gain with the position of the p-n junction in the avalanche region.

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As the depth increases, the avalanche gain also increases, but this also reduces the voltage margin that is available to operate the device below the break down voltage.

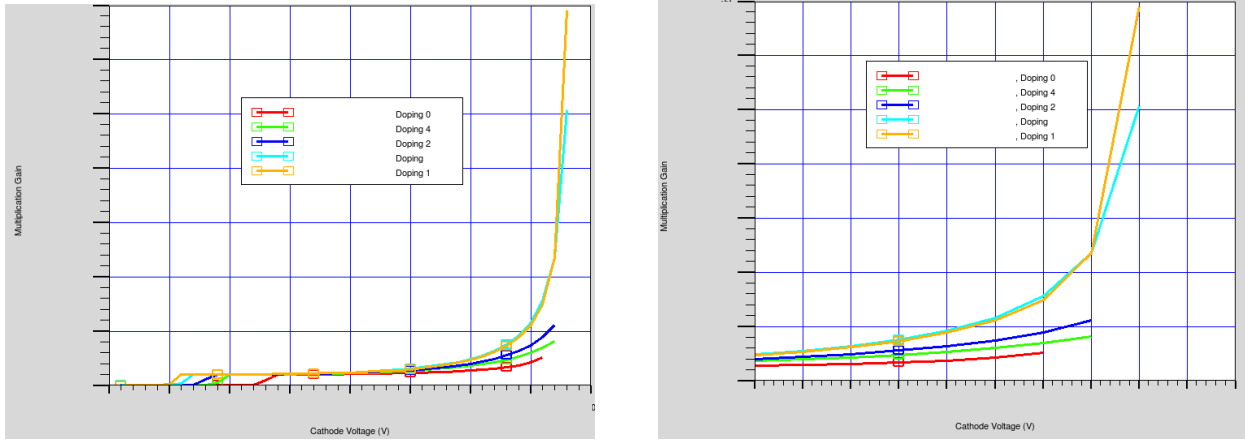


Figure 4. Simulated Gain results of a back-illuminated InP/InGaAs avalanche photodiode with variation of p-n junction depth in the multiplication layer.

Figure 5 shows the simulated dark and photo- current variation as a function of reverse bias voltage of the planar InP/InGaAsP based avalanche photodetector. As seen from this figure, the punch-through and break down voltage is strongly dependent on width of the multiplication region. Also shown in Figure 5 is the intensity distribution inside the device. The input beam diameter and pixel pitch are swept to better understand the crosstalk between neighboring pixels. From these simulations, the trench depth width and depth requirements were extracted.

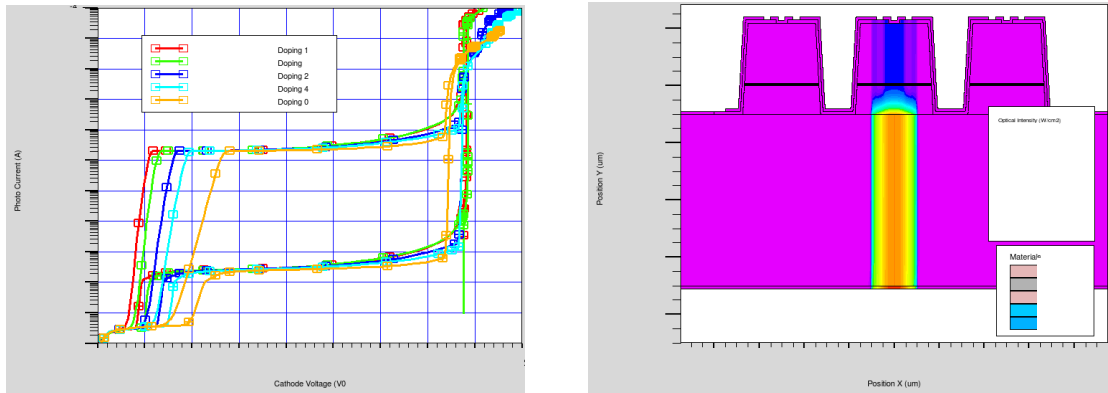


Figure 5. Simulated dark and photo current of a back-illuminated InP/InGaAs avalanche photodiode with variation of p-n junction depth in the multiplication layer.

4. EXPERIMENTAL RESULTS

Figure 6 shows the measured dark and photo- current variation as a function of reverse bias voltage. As seen from a comparison of Figures 5 and 6, the measured dark and photo- current variation with reverse bias voltage tracks the simulated dark and photo- current variation. Also, shown in the Figure 6 is the measured gain as a function of reverse bias voltage.

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Figure 7 shows the frequency response characteristics of the InP/InGaAsP device structure shown in Figure 1. The device response has a flat frequency response up for moderate bandwidths (e.g. > 5 GHz). Also shown in Figure 7 is the optical beam ray distribution along the beam path for a narrow (e.g. < 5 μm) beam diameter to better understand the optical crosstalk and interface reflections with in the device.

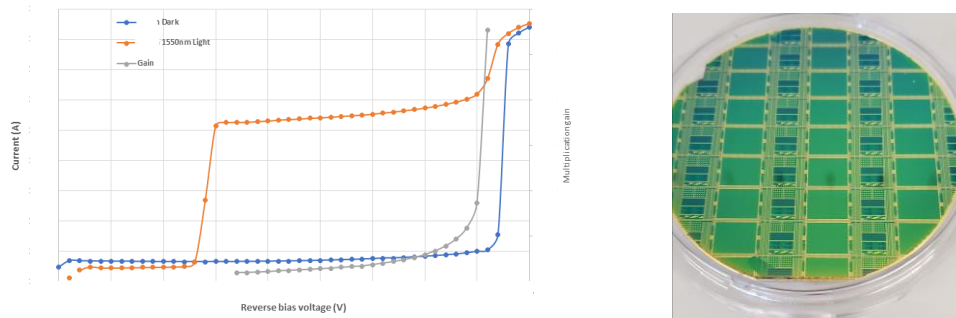


Figure 6. Measured dark and photo current and Gain of a fabricated back-illuminated InP/InGaAs avalanche photodiode pixel. Also shown is the top view of the fabricated wafer.

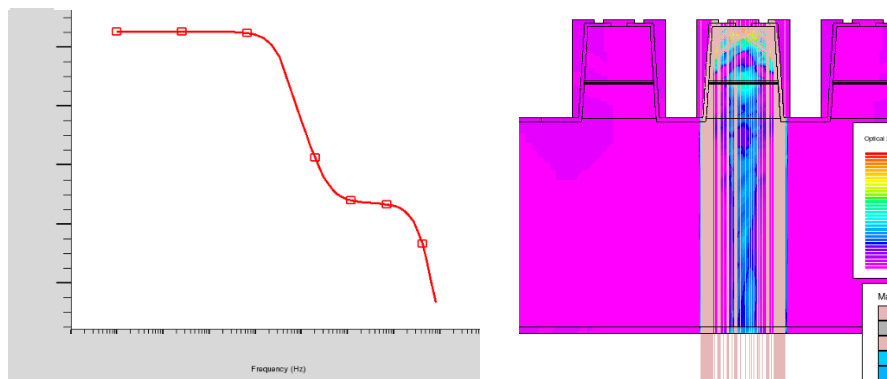


Figure 7. Simulated frequency response and optical intensity distribution of a back-illuminated InP/InGaAs avalanche photodiode pixel.

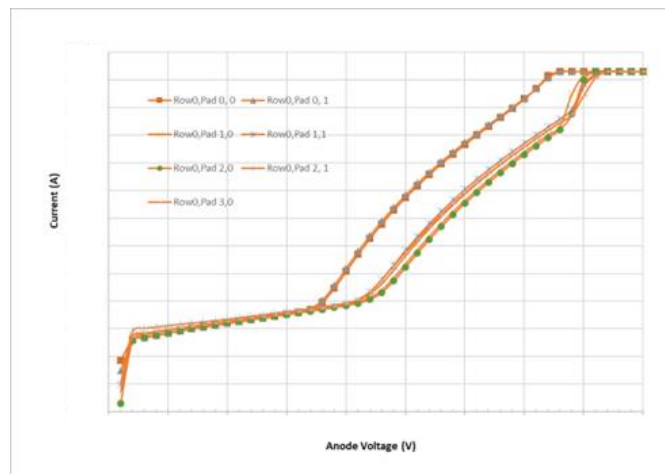


Figure 8. Measured break down voltage uniformity on a 3'' wafer.

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4.1 Breakdown voltage uniformity

Figure 8 shows the measured breakdown voltage variation on a fabricated 3” wafer. As seen from Figure 8, the breakdown voltage variation is < 3% for the detector test structures probed from left to right and top to bottom of the wafer for two different variations of the pixel device construction. In both directions, the breakdown voltage uniformity is less than 3% on a 3” wafer indicating excellent fabrication process control.

4.2 Geiger Mode Simulation

To optimize the avalanche photo diode design for Geiger mode operation, we have carried out extensive device simulations. In our simulation method Geiger mode performance is ascertained by the calculation of the single photon, single electron, or single hole probability of avalanche breakdown spatially in the device. These calculations are done using line integrals as suggested by McIntyre [13] of ionization rates along the paths of steepest potential gradient. These calculations are done as a post processing step after convergence is obtained with out any impact ionization or thermal models. To enable the post processing in Geiger mode, one must first probe the value of probability of avalanche due to introduction of an electron, hole or electron-hole pair. The calculation method is like the method of ionization integrals used to determine breakdown voltage, in which ionization rates are integrated along electric field lines from anode to cathode. In this case, however, the integrals along the field lines involve the probabilities of avalanche initiation and are used to solve the following set of equations:

$$dP_e/ds = (1 - P_e) \alpha_e P_p \quad (1)$$

$$dP_h/ds = (1 - P_h) \alpha_h P_p \quad (2)$$

$$P_p = P_e + P_h - P_e * P_h \quad (3)$$

where $s(x,y)$ is the distance along the field line, $P_e(x,y)$ is the probability that an electron generated at (x,y) will initiate an avalanche, $P_h(x,y)$ is the probability that a hole generated at (x,y) will cause an avalanche, and $P_p(x,y)$ is the joint probability that an electron-hole pair generated at (x,y) will initiate an avalanche event. α_e and α_h are the electron and hole ionization rates. Figure 9 shows the simulated electron and hole avalanche probability of the device structure shown in Figure 1. More than a 70% probability of avalanche is achieved with a moderate over voltage (e.g. > 1V).

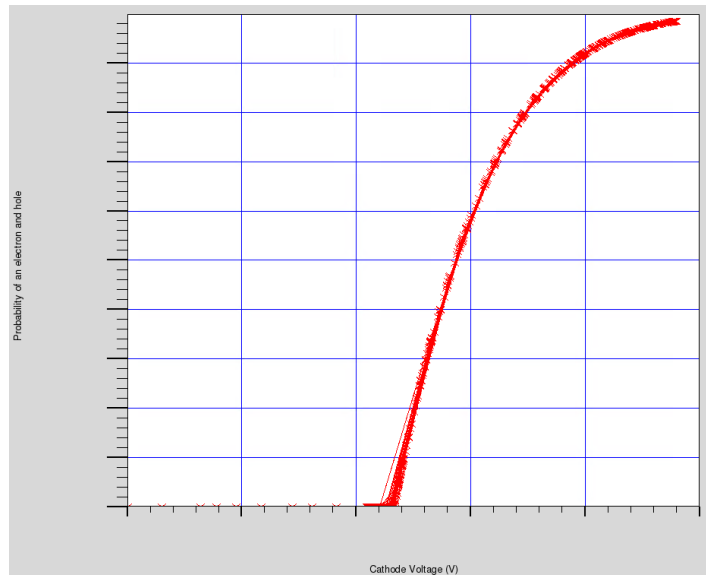


Figure 9. electron/hole avalanche probability in the device structure shown in Figure 1.

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The Photon Detection Efficiency (PDE) is the product of three parameters:

$$\text{PDE}(\lambda) = F_f * \eta(\lambda) * \varepsilon(V) \quad (4)$$

where F_f is the fill factor, $\eta(\lambda)$ is the quantum efficiency and $\varepsilon(V)$ is the avalanche initiation probability, which is a function of the bias voltage.

Figure 10 shows the PDE simulation results of the pixel architecture shown in Figure 1. The simulated PDE is greater than 35% for a moderate (e.g. > 1V) over voltage operation in Geiger mode. As expected, the PDE increases with the increasing operating voltage.

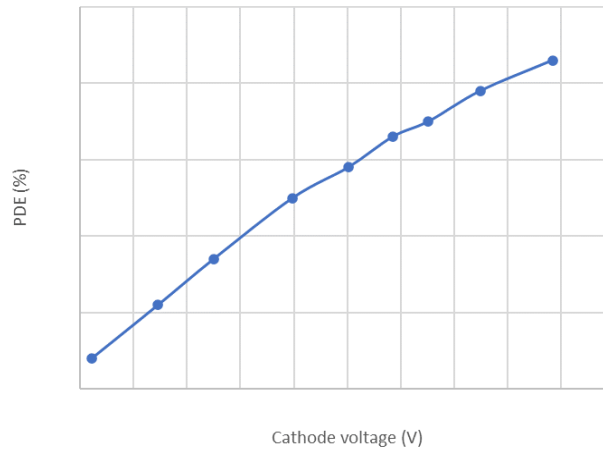


Figure 10. Simulation results of Photon Detection Efficiency (PDE) of GMAPD device.

4.3 Discrete Quenching Circuits

The reliability of GMAPDs increased with the introduction of active quenching circuits [14]. By sensing the rise of the avalanche and actively quenching it, these architectures force the quenching and reset operations in relatively short time (few nanoseconds). This innovation ultimately paved the way for single-photon counting and time synchronized single-photon counting applications. Additionally, with the progress in miniaturizing feature sizes in CMOS processes, the supporting finer pitch pixel circuitry and hybridization technologies were also developed [15]. Fully dedicated and flexible fabrication provided best-in-class performance in terms of detection efficiency, noise, and jitter. However, to date, the lack of realizing fine processing control has limited the size of GMAPD arrays to large pitches (25 – 50 μm) and small formats (< 128x128). Improvements in hybridization techniques using modern flip chip technologies enabled the integration of medium-to-large format GMAPD sensor arrays. SUI has fabricated large format (> 128x128) and fine pitch (< 25 μm) GMAPD detector arrays.

SUI's approach to testing single pixel GMAPD detectors requires a discrete, component-based quenching circuit. SUI has developed two variants: one utilizing a comparator and PMOS discriminator circuit as shown in Figure 11 and the other using a high-speed operational amplifier (OPAMP) and comparator as shown in Figure 12. The comparator and PMOS-based circuit is limited by the bandwidth of the comparator whereas the OPAMP-based circuit is not. However, the OPAMP-based circuit requires a larger voltage swing to detect the changes at the differential input, which ultimately manifests itself as slower operation. When fully optimized, both circuits are expected to achieve the required performance to characterize the optimal performance of SUI's GMAPDs.

Figure 13 shows the measured dark and photon count rates measured at room temperature. The measured photon count rate is competitive (e.g. > 200 kHz) at room temperature and is limited by the bandwidth of the comparator. The measured dark count rate is also competitive (e.g. < 200 kHz) at room temperature for a large (e.g. > 25 μm) diffusion diameter test structure.

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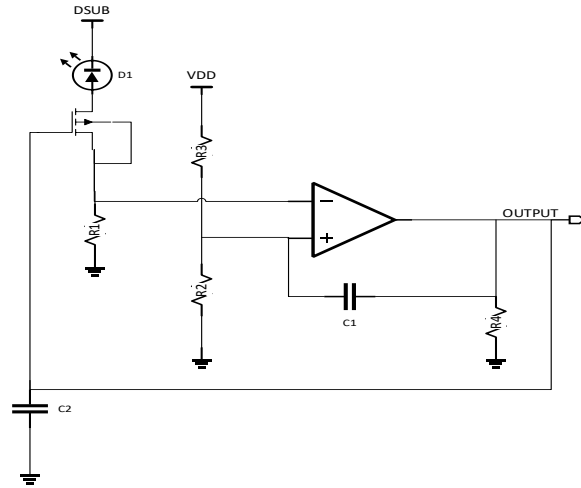


Figure 11. Quenching circuit using the comparator and PMOSFET as discriminators.

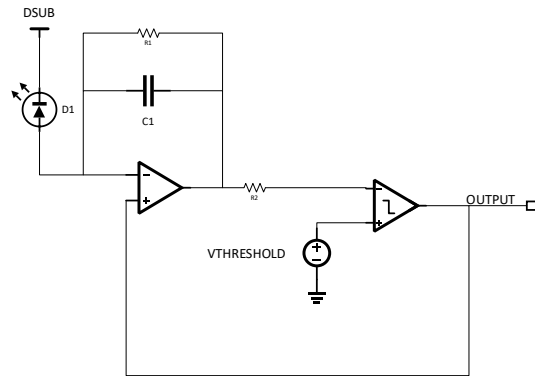


Figure 12. Quenching circuit using the comparator and OPAMP as discriminators.

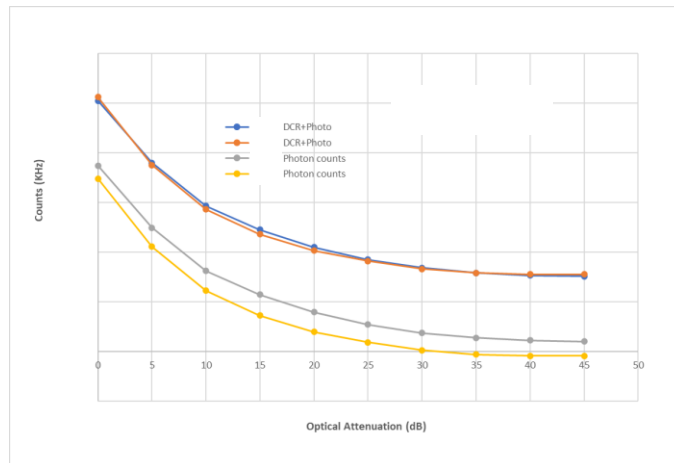


Figure 13. Measured GMAPD dark and photon counts using the discrete quenching circuit shown in Figure 11.

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4.4 CMOS Implementation of Quenching Circuit

The ability to detect single photons is becoming an enabling key capability in an increasing number of fields. Indeed, its scope is not limited to applications that specifically rely on single photons, such as quantum imaging, but also extends to applications where a low signal is overwhelmed by background light, such as in laser ranging applications. Recently silicon-based Single Photon Avalanche Photon Detectors (SPADs) gained popularity because of their small size; their capability to be monolithically integrated with a supporting readout integrated circuit similar to that of PIN-based sensors; their room temperature operation; their relatively low breakdown voltage; and, above all, their capability to be fast-gated (i.e. to time filter the incoming signal), which facilitates precise timestamping of the detected photons. The development of large digital arrays that integrates the detectors and circuits has allowed the implementation of complex functionality on-chip, tailoring the detectors to suit the needs of specific applications.

One such pixel design is shown in Figure 14. This monolithic CMOS quenching and amplification/digitization pixel circuit implementation is hybridized with the above discussed SWIR GMAPD detector array. The detector operating voltage will be adjusted through VQUENCH. The digital output, SPAD_out, of each pixel will be conveyed to readout circuitry.

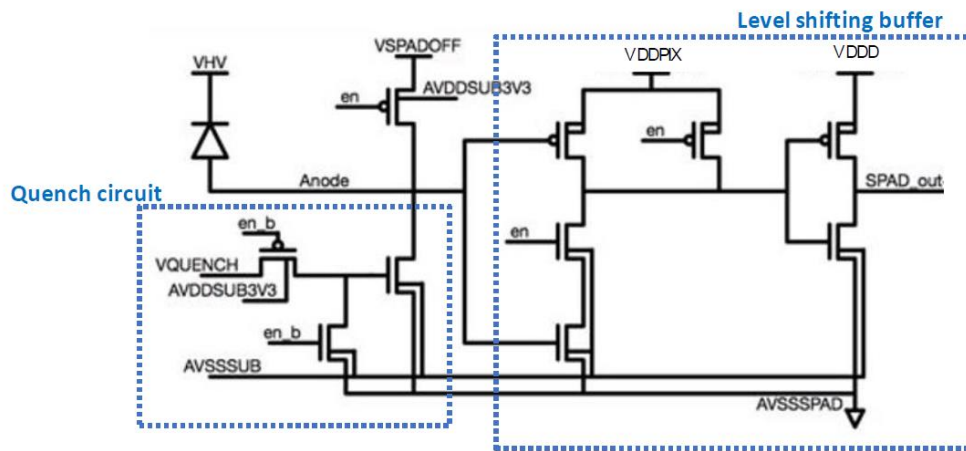


Figure 14. CMOS implementation of in-pixel quenching circuit.

5. CONCLUSIONS

We have proposed an InP/InGaAsP planar Separate Absorption Gain, Charge and Multiplication (SAGCM) region linear and Geiger mode avalanche photodetector and photodetector arrays using matured Metal Organic Chemical Vapor Deposition (MOCVD) epitaxial growth as well as other fabrication processes. We have developed TCAD models to simulate InP/InGaAsP materials-based avalanche photodetectors operating in Geiger-mode (GM), presented the simulated and experimental electro-optical performance results including the crosstalk between the neighboring pixels to improve the Modulation Transfer Function (MTF). The fabricated APD devices exhibit low dark current (e.g. < 5 pA) at an operating voltage between punch-through and breakdown with moderate gains (e.g. > 20) and moderate bandwidths (e.g. > 6 GHz in this linear mode; and these same devices exhibit moderately low (e.g. < 200 kHz) dark count rate and moderately high (e.g. > 300 kHz) photon count rate for larger (e.g. > 25 μm) test structure devices. Also presented are both the discrete and CMOS implementation of quenching/pixel circuitry that have been or will be hybridized with fabricated GM-APD detector arrays. The above results support that the InP/InGaAsP based device structure that we have developed has yielded device characteristics that are sufficiently good for practical and accurate time-of-flight (ToF) range measurements and as well as low-light imaging applications. We intend to integrate these detector arrays with the custom Read Out Integrated Circuit (ROICs) that are simultaneously being developed at SUI, Raytheon Technologies.

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