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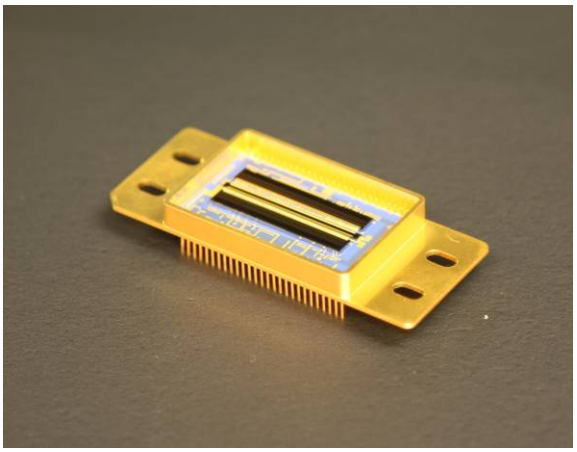
LC Series

Linear Indium Gallium Arsenide Photodiode Arrays



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In this datasheet, the use of all capital letters when referring to a signal usually signifies that there is an I/O pin on the product package connected to that signal, e.g., VREF.

1 Features

- Four integration capacitors: 0.13 pF, 1.0 pF, 10 pF and 20 pF
- Autozero for lower detector dark current and dark non-uniformity.
- Serial input for mode control
- Antiblooming to prevent charge overflow from saturated pixels
- Snapshot integration for simultaneous exposure of all pixels
- External control of integration timing for nondestructive readout
- High line rate readout:
  - 12.5 MHz maximum clock frequency
  - 1, 2, 4 or 8 outputs, depending on the configuration and mode
  - Integrate-while-read operation
- Wavelength ranges:
  - Raman wavelength range of 0.8 to 1.45 µm
  - Standard wavelength range of 0.8 µm to 1.7 µm
  - Extended wavelength range of 1.0 µm to 2.2 µm
  - Extended wavelength range of 1.0 µm to 2.6 µm
- Potential Configurations (not all variations and wavelengths combinations in production):
  - SU1024LC: 1024 pixels on a 25 µm pitch
  - SU512LC: 512 pixels on a 25 µm pitch
  - SU512LSC: 512 pixels on a 50 µm pitch
  - SU256LSC: 256 pixels on a 50 µm pitch
  - Available with or without 1 or 2 stage thermoelectric coolers

2 Principles of Operation

This linear focal plane array (FPA) is a hybrid combination of an InGaAs photodiode array and silicon CMOS readout integrated circuits (ROICs). The ROICs are "active pixel" devices in which the photocurrent is buffered, amplified and stored. A conceptual schematic is shown in Figure 1 and a timing overview is in Figure 2.

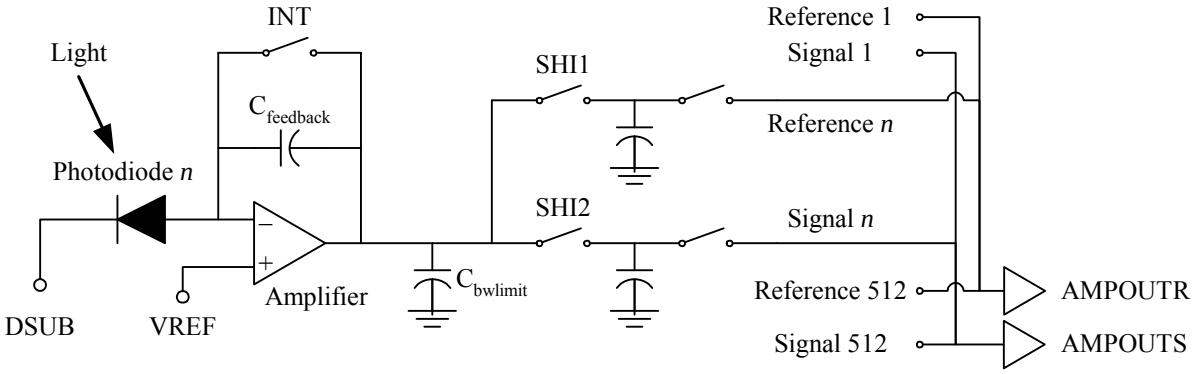


Figure 1. Conceptual schematic.

Each readout pixel contains a capacitive transimpedance amplifier (CTIA) with the photodiode at the input and the photodiode current integrated on a feedback capacitor. Four values of the feedback capacitance can be selected through the serial input (0.13 pF, 1 pF, 10 pF and 20 pF). In CTIA readouts, a larger capacitance provides greater charge storage capacity and dynamic range at the expense of lower sensitivity. The choice of the capacitance should therefore be interpreted as a choice between highest dynamic range at one end and highest sensitivity at the other.

Ideally, there is no bias or a slight reverse bias across the photodiodes. Referring to Figure 1, the level of this zero bias is set at VREF. In this series of arrays, VREF is set to 3.25 V by an external supply. Due to nonuniformity in the readout, however, the actual bias across the diodes can vary by ±3 mV when the autozero feature is disabled. Each pixel, therefore, will exhibit a dark current of $\Delta I = \Delta V/Ro$; the input offset voltage of that pixel divided by that

pixel's shunt resistance. As ΔV can vary between positive and negative, ΔI can be positive or negative. This is fixed for each pixel and the dark current due to this offset appears as a fixed pattern in the output which extends both positively and negatively from VREF. The light induced photocurrent ('signal') will drive the output negatively from VREF. Linear operation of the pixel is specified when the output signal is limited to be within the range of 2 V negative and ½ V positive relative to VREF. This means that following circuits should be designed to accept a range of 1.25 V to 3.75 V, with 1.25 V representing saturation by the combination of light induced photocurrent and dark current and the 3.75 V level representing saturation by positive going dark current. For valid averaging, ADC circuits should be designed to capture the full 2.5 V range and exposure times limited to avoid either saturation limit.

There are two sample-and-hold circuits at the output of the each pixel's CTIA: SHI1 and SHI2. This allows the array to operate in a parallel-in, serial-out "snapshot" mode. Between exposures, all of the pixels are held in reset then released so that the reference levels can be captured with the first sample-and-holds, SHI1. Following the exposure time, the signal levels are captured with the second sample-and-hold, SHI2. The pixels are then read out sequentially. Both the initial reference level (AMPOUTR) and the final signal level (AMPOUTS) will deviate from VREF with bipolar dark current and negative-going photocurrent. Integrate-while-readout operation is implemented with a second set of sample and holds in each pixel (SHI1' and SHI2'), that alternate with the first set (SHI1 and SHI2) to sample the integrated signal (n) for one readout and to hold the previous integration (n-1) for the current readout.

In a typical application, signal outputs AMPOUTR and AMPOUTS can be differentially amplified as a form of correlated double sampling (CDS). This eliminates much of the integrator reset related switching noise for the larger gain capacitances. This reset noise may be small for the smallest capacitor and CDS may result in more noise than just reading SHI2. Also note that the differential output will 'foldover' if the VIDEO2 signal saturates and the light intensity continues to increase, causing the VIDEO1 signal to also increase. The general line timing sequence is shown in Figure 2.

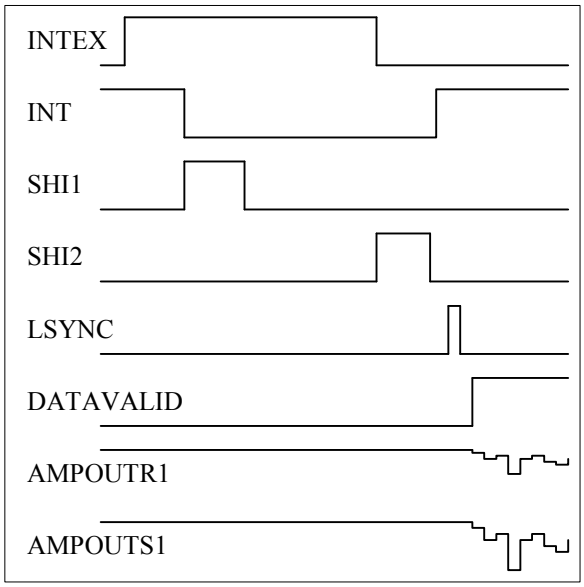


Figure 2. Timing overview.

Within each pixel, photocurrent is integrated for a period of time that is determined by the width of the INTEX pulse. While waiting for a line sequence to be initiated, the CTIA feedback capacitors are held in reset. Upon initiation by the rising edge of INTEX, the following events occur automatically:

- The INT switch is opened, which allows charge to integrate on the feedback capacitor.
- SHI1 (or SHI1') is activated to sample the reference voltage at the start of integration for 38.5 clock cycles (see Section 4.1). The reset charge on the capacitor, some signal light, and some dark current will be captured.
- Charge continues to integrate on the feedback capacitor.

When the line sequence is terminated by the falling edge of INTEX, the following events occur automatically:

- SHI2 (or SHI2') is activated to sample the signal voltage at the end of charge integration.
- The INT switch is closed, draining charge from the feedback capacitors.
- The shift registers begin operation so that the pixel-by-pixel signals, at the beginning of (SHI1 or SHI1') and at the end of integration (SHI2 or SHI2'), appear at AMPOUTR and AMPOUTS sequentially.

All of the above functions are generated internally. The user need only provide a continuous master clock (CLOCK) and a line-trigger pulse (INTEX). The array also supports an external timing mode, where the user has direct control over all the timing signals. To implement correlated double sampling, the Video 1 and 2 signals should be buffered with low-noise, low-offset buffers and those outputs connected to the inputs of a low-noise differential operational amplifier.

Devices from the LC family with photodiodes at 25-micron pitch have a separate pair of Video 1 and 2 outputs for the odd and the even pixels. When viewing the package from the top with pin 1 oriented to the top left, the right-side output reads the odd pixels and the left-side outputs read the even pixels. As the odd and even pixels are read out through separate circuits, the gain and offsets of those circuits will not be the same. This will usually result in an electrical odd-even pattern in the readout signal, in addition to the fixed pattern of the photodiode and CTIA variations. The LC ROICs have up to 4 outputs each, so users may observe a repeated pattern of 4 or 8 variations, again due to differences in the independent output circuits. For stable environmental conditions and exposure times, the fixed patterns will be quite stable. The offset variations may be minimized with simple background subtraction of an averaged set of dark scans. The amplifier gain and photodiode non-uniformity of response variations, along with the dark fixed pattern, may be removed by implementing a simple two point correction using a linear fit between the dark response and uniform illumination at a set level of illumination such as at 50% of full scale. The device response for each pixel is linear, so stored corrections, based on averaged data to remove temporal noise, is quite effective. Single-output arrays, such as the LSC type, only have one set of amplification circuitry and therefore do not exhibit an electrical odd-even variation. See section 13.5 for a discussion of optical odd-even that can occur for the pixels with heights of 50, 250 or 500 µm. The square pixel 25-µm-high aperture arrays are created with a photomask on the top surface of the photodiode arrays creating a sharp and even edge across all diodes, minimizing the potential for optical odd-even response variations.

3 Operation

3.1 DC Power Supplies and Bias Voltages

There are separate power supplies for digital and analog circuits. The positive power supplies of each type should be connected together external to the package and bypassed with a 1-µF tantalum capacitor in parallel with a few 0.1-µF ceramic chip capacitors. The digital and analog common should be tied together where they connect to the printed circuit board and connect to the system analog ground. Pin 14 of the device is connected to the case and should be connected to earth ground while avoiding ground loops to supply or signal grounds.

3.2 Clocks

If programmable logic is used to generate input clocks (such as CLOCK and INTEX), a 100 Ω resistor should be in series with each clock line and mounted as close to the source as possible. This will suppress ringing in the clock edges. CLOCK should run continuously to allow internal timing functions to operate properly.

3.3 VREF, DSUB and GUARD

VREF and voltages referenced to VREF are shown in Figure 3, with the definitions

- Vdsub = DSUB – VREF
- Vguard = VREF – GUARD.

VREF is the reference voltage for the transimpedance amplifier, and is supplied by the user. Any noise or shift in VREF has unity gain to the output, so the stability of VREF is particularly important for low noise and for good

autozero performance. The greatest demand on VREF is during the autozero sampling, which occurs before the integration and lasts for a minimum of 7.2 µs (due to the restriction of the clock rate to => 5 MHz for this mode) with up to a 7-nF load. It is recommended for the VREF supply to have an output impedance less than 50 Ω for adequate slewing and to provide up to a 20-mA slewing current. To reduce noise, Cfilter is recommended to be a 1-µF tantalum capacitor in parallel with a few 0.1-µF ceramic chip capacitors.

DSUB is the connection to the photodiode substrate, and GUARD is the connection to the photodiode array guard lines above and below the imaging line. For photodiodes with a 250- or 500-µm aperture (sometimes called tall or rectangular pixels), Vdsub = 0 (i.e., Dsub = Vref) so the GUARD connection is not required (the GUARD pin has no internal connection for these tall pixel arrays). For photodiodes with a 25- or 50-µm aperture (called square pixels), Vguard = 200 mV ± 20 mV, and Vdsub must be set in the range of 0 to 25 mV (with a resolution of < 1 mV) to keep the array average dark output nominally at zero. This may need to be adjusted if the operating temperature is changed. The total photocurrent of the array flows through DSUB, so the GUARD may draw up to 10 mA.

With autozero on, for both square and tall pixels, it is also recommended to have a fine adjustment of Vdsub over the range of ± 1 mV with a 10 µV resolution. This adjustment allows for minimization of the dark current if there is a residual difference between VREF and DSUB in the nominal electronics design, particularly if the array will be operated cooled. NOTE: Vdsub = +75 to 100 mV reverse bias may reduce Johnson noise while at the expense of increasing dark current. It will also shift all of the pixel offsets to produce positive going dark current.

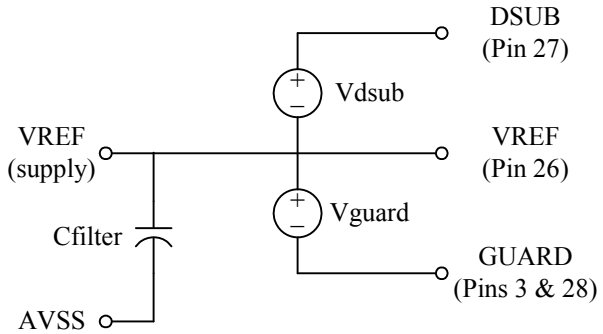


Figure 3. Recommended circuit for VREF referred inputs.

3.4 Power up Reset

Upon power up the user should reset the circuit by holding the RESETN signal low or sending a two-clock cycle wide high pulse to the SI pad (see §5.2). This will reset all of the digital circuits and set the analog circuits to be ready to begin integrating a new line. The RESETN is asynchronous but should be held low for at least 2 clocks to ensure proper device reset. The device is reset to the default mode 1 clock cycle after RESETN signal returns high. For normal operation, RESETN should be held high after the reset.

3.5 Video Output

- See Figure 4 for the readout configurations. For the two-sided arrays, odd pixels are connected to the outputs on the right side, and even pixels are connected to the outputs on the left side. For single-sided arrays, all the pixels output on the right side.
- The inactive pixel output level is set to a value nominally the same as VREF, as is the nominal dark level voltage for the output from active pixels. Due to variations in the integrator voltage offsets from pixel-to-pixel, dark current will grow from VREF in either direction. Photocurrent generated by light signal will drive the output to voltages below VREF, i.e., in the negative direction, with nominal full well capacity reached at -2 V from VREF.

- The CDS output is the difference between AMPOUTR (reference) and AMPOUTS (signal). The difference may be performed in the analog domain, or AMPOUTR and AMPOUTS may be individually digitized and the difference performed in the digital domain. Either way, the load should not exceed the maximum value in Table 10.

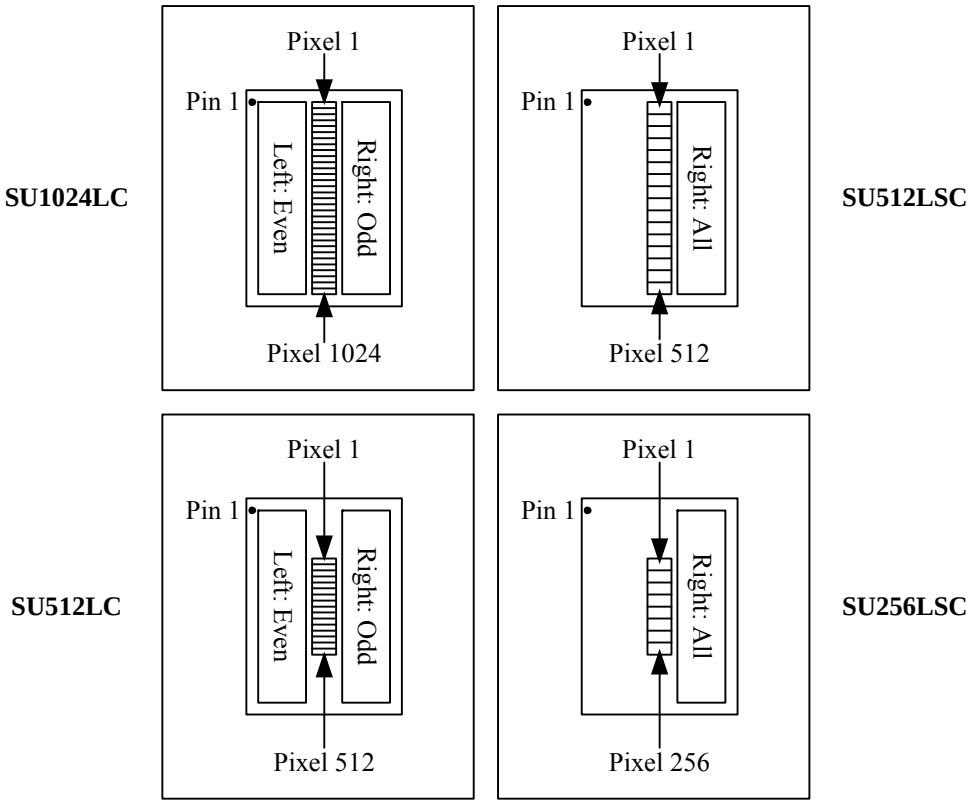


Figure 4. Readout configurations, top view.

4 Timing

In the default mode, CLOCK and INTEX are used to control integration time and readout. In external integration control mode (selected via the Serial Interface bit 10 – see section 5.1), the clocks EXSH1, EXSH2 and LSYNC_EX must also be supplied. The integration timing, the readout timing and the nondestructive reading timing are described in this section, followed by a calculation of the line rate. Note: Use of internal timing is recommended unless implementing nondestructive reading.

4.1 Integration Time Control

The timing of the pixel to control integration time is shown in Figure 5. The integration period begins when the first sample is complete (SHI1 falls) and it ends when the second sample is complete (SHI2 falls). When internal timing is used, the integration time is 38.5 clocks less than the positive width of the INTEX pulse, and is delayed 41 clocks from the rising edge of INTEX. When external timing is used, SHI1, SHI2 and LSYNC (internal) are controled by the corresponding inputs, and INTEX is still needed to reset the CTIA. The rise and fall times are approximately 20 ns.

- The minimum integration time is 2.92 µs (36.5 * 80 ns).
- The minimum reset time, INTEX low time, is:
  - Greater of 11 clocks and 0.88 µs (11 * 80 ns) for high power mode
  - Greater of 24 clocks and 4.80 µs (24 * 200 ns) for low power mode without autozero function
  - Greater of 60 clocks and 12.0 µs (60 * 200 ns) for low power mode with autozero function
- Switching between internal and external timing may lose a frame.
- The edges of INTEX, INT, and SHI1 occur at the falling edge of the CLOCK; those of SHI2 occur at the rising edge.

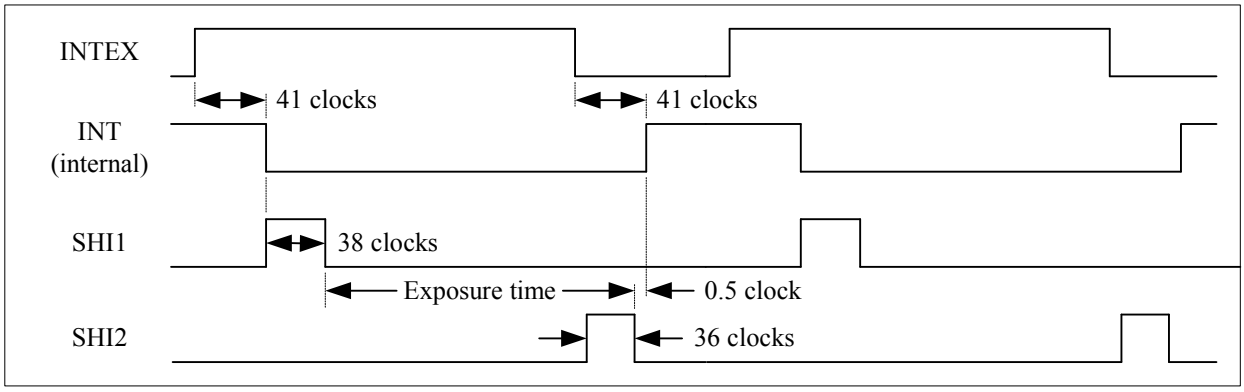


Figure 5. Integration timing.

4.2 Readout Timing

The timing of readout is shown in Figure 6. The readout sequence is started by the falling edge of INTEX, which generates an LSYNC with internal timing control. If external integration time control is used, LSYNC_EX simply is used instead of the internal LSYNC to initiate readout. It is possible to have multiple readouts for a single integration time, if the integration time is long enough. Readout timing is the same in forward or reverse scan.

- A minimum of 8 overhead clocks are required per line. The minimum line time is 136 clocks.
- Integrate-while-read operation occurs when the INTEX reset period (active low) is less than the sum of the readout time plus the minimum time as defined in Section 4.1, and integrate-then-read when INTEX is low for longer periods.
- The edges of INTEX, LSYNC and video output occur at the falling edge of the CLOCK.

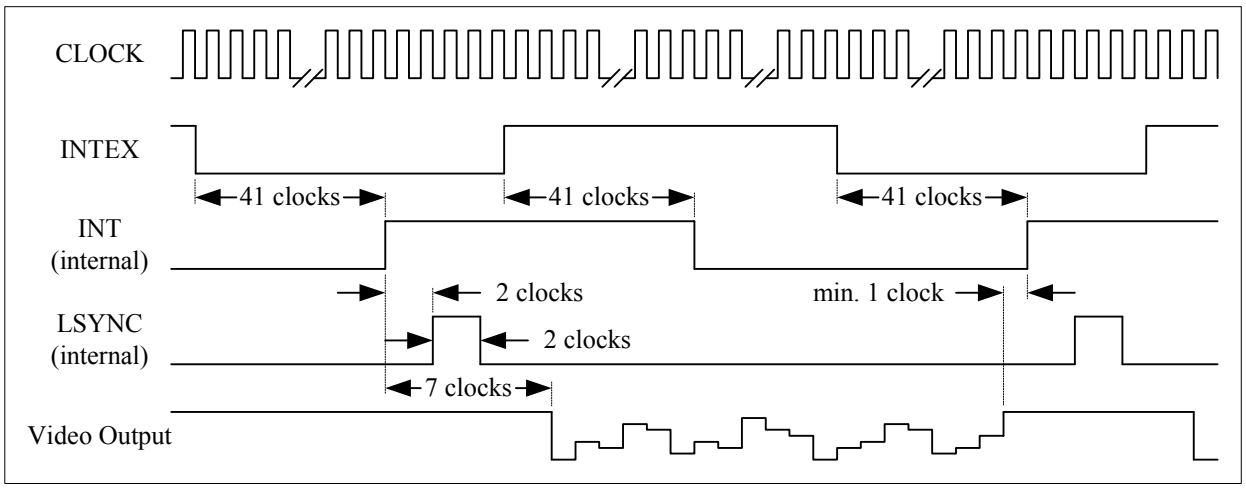


Figure 6. Readout timing.

The timing of the video output is summarized in Figure 7, where one pixel output occurs once per CLOCK period. The sampling for analog-to-digital conversion should occur just before the next falling edge of CLOCK to maximize the settling time.

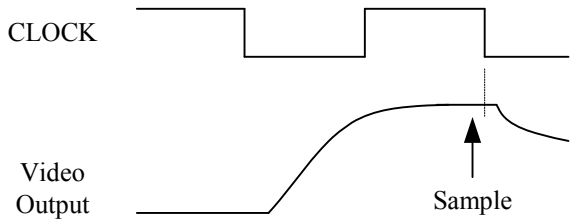


Figure 7. Single pixel video output.

4.3 Nondestructive read timing

Nondestructive read timing is shown in Figure 8.

- INTEX must stay high during the entire readout.
- The rising edge of the first sample is fixed at 41 clocks after the rising edge of INTEX.
- The duration from the previous falling edge of INTEX to the rising edge of LSYNC_EX controls the start of video output:
  - If the duration is an ***even*** number of clocks, video output starts 5 clocks after LSYNC_EX rises.
  - If the duration is an ***odd*** number of clocks, video output starts 4 clocks after LSYNC_EX rises.
  - It is strongly recommended to use an ***even*** number of clocks.
- The duration from the end of video output to the rising edge of the next sample should be an odd number of clocks with a minimum of 1.
- Either the reference output (using EXSH1) or the signal output (using EXSH2) can be used, but not both. If the signal output is used, extra transitions are needed for INTEX before the useful integration is started as shown in Figure 9.

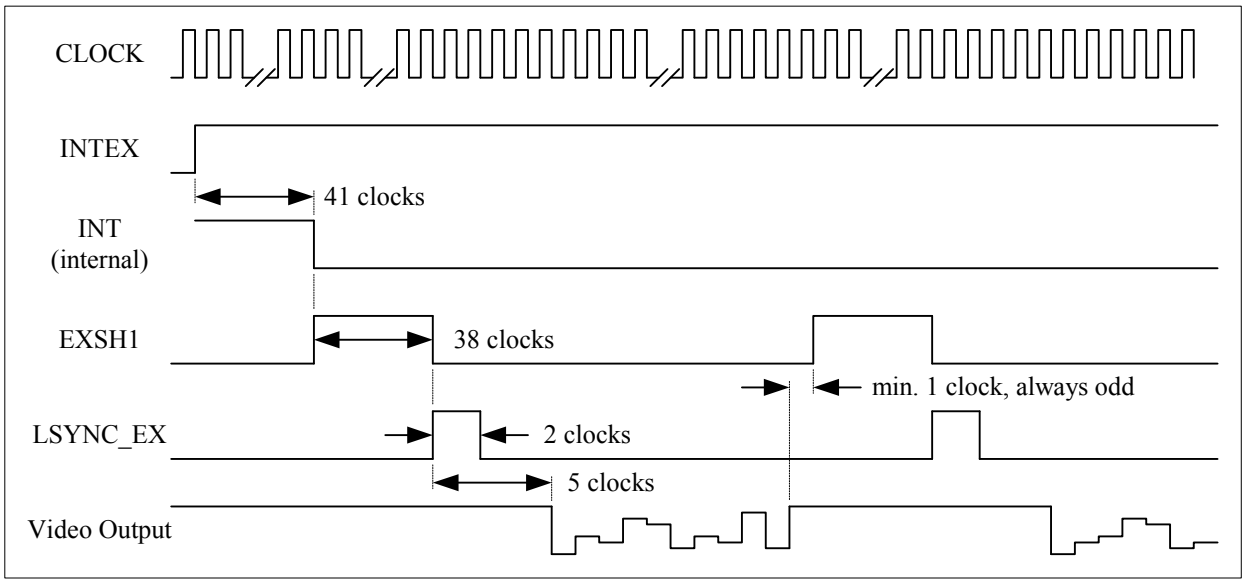


Figure 8. Nondestructive read timing.

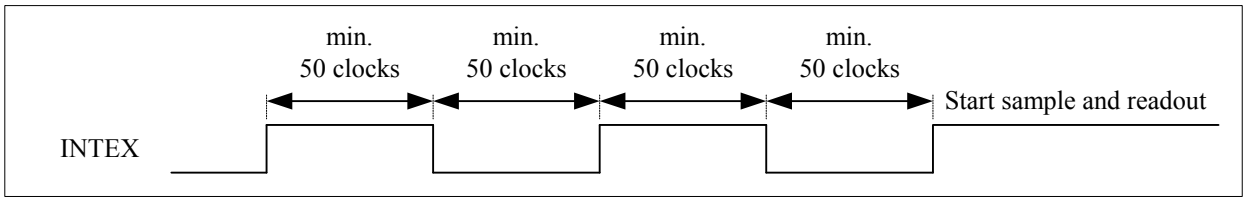


Figure 9. Extra setup timing required for the use of the signal output (using EXSH2).

4.4 Line Rate and Exposure Time Calculations

The line rate is determined by combining the readout timing requirements and the integration timing requirements. To obtain a high line rate, the ROIC is designed to allow integrate-while-read timing. Assuming that the line rate is limited by the readout and not the integration, the minimum line time is

$T_{LINE, MIN}$ = maximum (136, pixels/outputs + 8) * $T_{CLOCK} \geq 10.88$ µs

where $T_{CLOCK} \geq 80$ ns. The maximum line rate for each combination of window and output mode is listed in Table 1. Note that when multiple outputs are used the frame rate increases by less than a factor of two or four due to the constant overhead time.

Array and outputs	Minimum line time	Maximum line rate
SU512LSC, 1 output and SU1024LC, 2 outputs	(512 + 8)*80 ns = 41.60 µs	24.038 kHz
SU512LSC, 2 output and SU1024LC, 4 outputs	(256 + 8)*80 ns = 21.12 µs	47.348 kHz
SU512LSC, 4 output and SU1024LC, 8 outputs	(128 + 8)*80 ns = 10.88 µs	91.912 kHz
SU256LSC, 1 output and SU512LC, 2 outputs	(256 + 8)*80 ns = 21.12 µs	47.348 kHz
SU256LSC, 2 output and SU512LC, 4 outputs	(128 + 8)*80 ns = 10.88 µs	91.912 kHz
SU256LSC, 4 output and SU512LC, 8 outputs	Minimum line time allowed = 10.88 µs	91.912 kHz

Table 1. Line rates for a 12.5 MHz clock frequency.

The maximum exposure time for a given line time is

$$T_{EXPOSURE, MAX} = T_{LINE} - T_{MIN\ INTEX\ LOW} - 38.5 * T_{CLOCK}$$

where the minimum times for INTEX low are from Section 4.1and exposure times for the minimum line times are listed in Table 2.

Mode	Minimum line time	Maximum exposure time	Minimum exposure time
High power	136 * 80 ns = 10.88 µs	(136 – 11 – 38.5) * 80 ns = 6.92 µs	36.5 * 80 ns = 2.92 µs
Low power, autozero disabled	136 * 200 ns = 27.2 µs	(136 – 24 – 38.5) * 200 ns = 14.7 µs	36.5 * 200 ns = 7.3 µs
Low power, autozero enabled	136 *200 ns = 27.2 µs	(136 – 60 – 38.5) * 200 ns = 7.5 µs	36.5 * 200 ns = 7.3 µs

Table 2. Maximum exposure times for minimum line times.

The line time increases when either the exposure time exceeds the maximums listed in Table 2 or the INTEX low time is increased beyond the minimum. Integrate-then read timing is chosen by selecting the INTEX low time long enough to prevent the start of the next integration before the readout finishes.

The reference always consumes part of the integration time. For exposure times much longer than the minimum, the reference sample time is negligible. For the minimum exposure times, the reference is slightly more than half the total sampling time. This decreases the dynamic range by reducing the effective full well capacity of the integration circuit. It also results in a "fold-over" behavior, where the output signal decreases after the signal saturates and the reference continues to increase (until the reference also saturates).

This section assumes one read per integration. For the special case of nondestructive read mode, see Section 5.8.

5 Modes

The serial interface loads a register used to select the modes. The serial interface is described first, followed by each of the modes.

5.1 Serial Interface

The serial register begins loading following a one-clock cycle wide start bit on the SI pad (V_{IH}). The register should be loaded with a data rate equal to the clock rate and transition on the falling edge of the clock. This can be done whenever a change in operation is desired or after a RESET, except during the falling edge of INTEX. It is not necessary to reassert the write on every INTEX, but permissible to do so. Reserved bits should be loaded with a logical 0. Figure 10 shows the timing for loading the serial register, and Table 3 lists the bit definitions. In particular,

- The commands are effective as follows:
  - The reset bit takes effect one clock later than applied
  - The other bits take effect a few nanoseconds later than the falling edge of INTEX.
- The SI may be loaded at any time with the following restrictions:
  - Bit 0 ends at least 2 clocks earlier than the falling edge of INTEX
  - Bit 16 starts at least 1 clock later than the falling edge of INTEX.

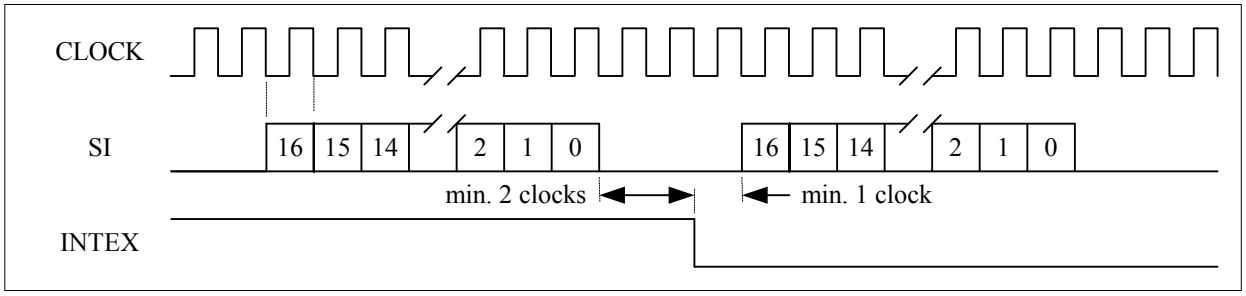


Figure 10. Timing of serial register loading.

Bit	Function	Description	Default (1 = V_{IH};; 0 = V_{IL})
0	Reserved		0
1	MD_ANTI_BLMB	Antiblooming disable	0, enable
2	NON_DESTRUCTIVE	Nondestructive read enable	0, disable
3	Reserved		0
4	HIGH_POWER	High power enable	0, low power
5	IBCAP1	Bandwidth limiting capacitance	00, 1.5 pF (minimum)
6	IBCAP0		
7	FCAP1	Feedback capacitance	00, 0.13 pF (high gain)
8	FCAP0		
9	AUTOZEROB	Autozero disable	0, enable
10	EXTERNAL_INT	External timing control enable	0, internal
11	Reserved		0
12	Reserved		0
13	OUTSLT1	Output selection	00, 1 output
14	OUTSLT0		
15	RESET	Reset internal registers	0, inactive
16	START	Start loading serial register	0, inactive

Table 3. Serial register bit definitions.

5.2 Reset

The reset function puts the configuration into a known state, with the following two options:

- RESETN (pin 36) pulsed low (V_{IL}) resets all internal registers and all bits in the serial word register.
- The reset bit entered into the serial interface input resets all registers except the serial word register.

5.3 Multiple Outputs

Output selection via the serial work register is shown in Table 4, where one output per ROIC is the default. Two or four outputs per ROIC may be used in order to achieve higher frame rates. Every 8 pixels per ROIC form a group:

- In 2-output mode, the first 4 pixels in each group go to output 1 and the last 4 pixels go to output 2.
- In 4-output mode, the first 2 pixels in each group go to output 1, the second 2 pixels go to output 2, etc.

This rule is applied to all configurations in Table 5, where arrays with two ROICs interleave the odd and even photodiodes between the right and left outputs (respectively).

Output Select 1	Output Select 0	Outputs per ROIC
0	0	1 (default)
1	0	2
0	1	4
1	1	4

Table 4. Output selection control bits in serial word register.

Configuration	Output	Clock 1	Clock 2	Clock 3	Clock 4	Clock 5	Clock 6	Clock 7	Clock 8
SU256LSC or SU512LSC 1 output – 50 µm pitch	1 Right	1	2	3	4	5	6	7	8
SU256LSC or SU512LSC 2 outputs – 50 µm pitch	1 Right	1	2	3	4				
	2 Right	5	6	7	8				
SU256LSC or SU512LSC 4 outputs – 50 µm pitch	1 Right	1	2						
	2 Right	3	4						
	3 Right	5	6						
	4 Right	7	8						
SU512LC or SU1024LC 2 outputs – 25 µm pitch	1 Right	1	3	5	7	9	11	13	15
	1 Left	2	4	6	8	10	12	14	16
SU512LC or SU1024LC 4 outputs – 25 µm pitch	1 Right	1	3	5	7				
	2 Right	9	11	13	15				
	1 Left	2	4	6	8				
	2 Left	10	12	14	16				
SU512LC or SU1024LC 8 outputs – 25 µm pitch	1 Right	1	3						
	2 Right	5	7						
	3 Right	9	11						
	4 Right	13	15						
	1 Left	2	4						
	2 Left	6	8						
	3 Left	10	12						
	4 Left	14	16						

Table 5. Correspondence between active video output and photodiode number.

5.4 External Integration Time Control

In external timing mode, selected by bit 10 of the Serial Interface register (see section 5.1), EXSH1 and EXSH2 simply replace SHI1 and SHI2 in Figure 5. LSYNC_EX replaces internal LSYNC in Figure 6. If external timing

will not be used, leave these input pins open. The external signals must still follow the timing constraints listed for the internal control signals.

5.5 Autozero

This mode reduces the dark current and dark non-uniformity by minimizing the CTIA offsets on each pixel during the time INTEX is low, A circuit to adjust the Vdsub difference between the DSUB and VREF signals, as described in Section 3.3, will permit negating the residual mean offset even further, particularly if the array will be cooled The Autozero mode is recommended for arrays with extended wavelength material (wavelength response cutoffs of 2.2 µm and 2.6 µm). The ROIC default operation is with Autozero on, and requires the following:

- INTEX low time >= 12 µs and 60 clocks
- Low Power mode selected in the serial interface register (see Section 5.1)
- Clock frequency <= 5 MHz.

5.6 Capacitor Selection

The capacitor selections are given in Table 6 and Table 7. The maximum clock frequency for selected combinations is given in Table 8.

FCAP 1	FCAP 0	Feedback capacitance (pF)	Capacity with 2 V output swing (Me)
0	0	0.1 (default)	1.25
1	0	1.0	12.5
1	1	10.0	125
0	1	20.0	250

Table 6. Feedback capacitor selection via serial word register.

IBCAP 1	IBCAP 0	Bandwidth limiting capacitance (pF)
0	0	1.5 (default)
1	0	3.0
1	1	10.5
0	1	50.5

Table 7. Bandwidth limiting capacitor selection.

Power Mode	Bandwidth limiting capacitance	Feedback capacitance	Maximum clock frequency
High power	1.5 pF	0.13 pF or 1.0 pF	12.5 MHz
Low power	1.5 pF or 3.0 pF	any	5.0 MHz
Low power	10.5 pF	any	1.4 MHz
Low power	50.5 pF	any	0.3 MHz

Table 8. Maximum clock frequency for selected mode combinations.

5.7 High Power

This mode should be used when any of the following are true:

- Clock frequency > 5 MHz
- SHI1 high duration < 7.6 µs
- SHI2 high duration < 7.2 µs

5.8 Nondestructive Read (NR)

The nondestructive read mode is intended for the use of techniques to reduce the read noise, such as up-the-ramp sampling. NR is achieved by disabling the alternating pairs of sample and holds in the pixel (see Section 2); therefore, reading out the previous line while integrating the present line is not allowed. LSYNC_EX and either EXSH1 or EXHS2 must be supplied for NR (The external integration time control mode is automatically used).

5.9 Anti-blooming

This mode prevents charge overflow from saturated pixels. The default is to enable anti-blooming.

6 Pin Assignments

The pin assignments are listed in Table 9 and shown in Figure 11. Unused inputs (NC) should be left unconnected.

The RT and LT versions have the same pinout as the T1, except that the RT and LT versions do not have a thermoelectric cooler (pins 1, 2, 53 and 54 are NC). The T1 version has pins 1 and 54 internally connected to the TE Cooler. The T2 version has doubled TE cooler connections that are required to manage the higher current flow through the two-stage cooler. Pins 1 and 2 are assigned for the TE Cooler (+), and pins 53 and 54 are assigned for the TE Cooler (-). The TE controller circuit should be designed to supply equal TE Cooler (+) power to pins 1 and 2, and equal TE Cooler (-) power to pins 53 and 54.

For single-sided arrays (SU256LSC and SU512LSC shown in Figure 4), the pins with a label ending in "left" are not used. To minimize noise coupling, pins without internal connection may be connected to a clean analog ground.

The GUARD connections (pins 3 and 28) are only required for photodiodes with a 25 or 50 µm aperture (height). For photodiodes with a 250 or 500 µm aperture, the pin is NC but it is acceptable to apply a bias if the circuit is to be designed to support both types of arrays.

Pin	Label	Pin	Label
1	TE Cooler (+) (T1 and T2) NC (RT and LT)	28	GUARD
2	NC (RT, LT and T1) TE Cooler (+) (T2)	29	DVDD right
3	GUARD	30	DVSS right
4	DVDD left	31	INTEX right
5	DVSS left	32	LSYNC_EX right
6	INTEX left	33	EXSH1 right
7	LSYNC_EX left	34	EXSH2 right
8	EXSH1 left	35	SI right
9	EXSH2 left	36	RESETN
10	SI left	37	DVDD right (logic high)
11	NC	38	NC
12	Temp. Sensor (-)	39	NC
13	Temp. Sensor (+)	40	NC
14	Case	41	CLOCK right
15	CLOCK left	42	AVSS right
16	AVSS left	43	AVDD right
17	AVDD left	44	AMPOUTR4 right
18	AMPOUTR4 left	45	AMPOUTS4 right
19	AMPOUTS4 left	46	AMPOUTR3 right
20	AMPOUTR3 left	47	AMPOUTS3 right
21	AMPOUTS3 left	48	AMPOUTR2 right
22	AMPOUTR2 left	49	AMPOUTS2 right
23	AMPOUTS2 left	50	AMPOUTR1 right
24	AMPOUTR1 left	51	AMPOUTS1 right
25	AMPOUTS1 left	52	NC
26	VREF	53	NC (RT, LT and T1) TE Cooler (-) (T2)
27	DSUB	54	TE Cooler (-) (T1 and T2) NC (RT and LT)

Table 9. Pin Assignments.

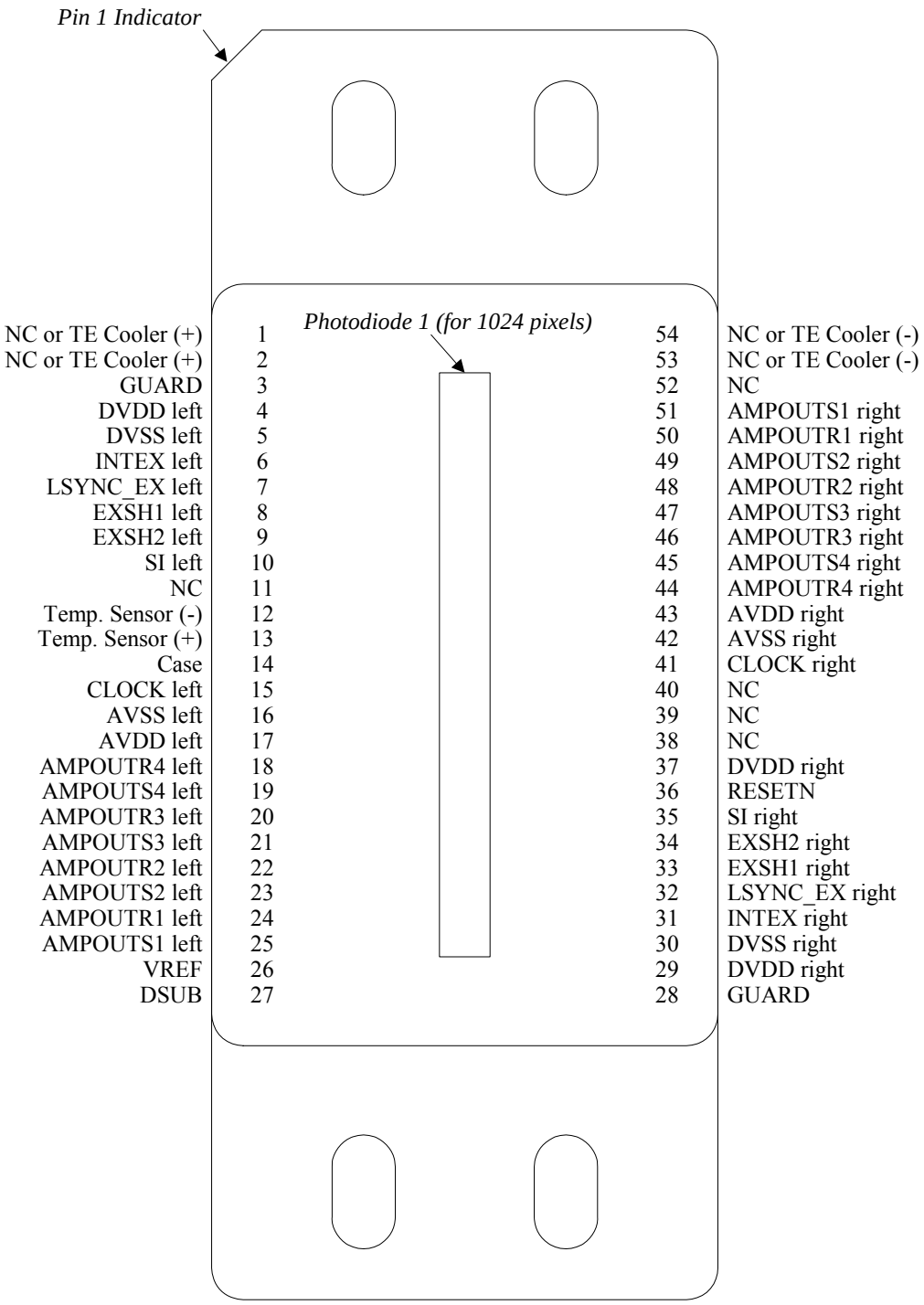


Figure 11. Pin diagram, top view.

7 Specifications

Conditions are the following, unless otherwise noted:

- Ambient Temperature = 20°C
- AVDD = 5 V and DVDD = 5 V
- Video output load = 100 kΩ, 20 pF
- Clock rate = 12.5 MHz
- Default Mode Operation

Parameter	Comments	Value			Unit
		Min	Typical	Max	
Power Supplies					
Supplies DVDD and AVDD		4.5	5.0	5.5	V
Grounds DVSS and AVSS		0.0	0.0	0.0	V
Power dissipation, analog	See Table 11				mW
Power supply ripple				0.250	mV
Biases					
VREF		3.15	3.25	3.35	V
VREF ripple				0.025	mV
V_{dsub} = DSUB - VREF	Aperture > 50 µm Aperture ≤ 50 µm Autozero on	0 0 -1	0 10 0	0 25 1	mV mV mV
V_{guard} = VREF - GUARD	Aperture ≤ 50 µm	0.18	0.20	0.22	V
I_{GUARD}	Aperture ≤ 50 µm			10	mA
Digital Inputs - INTEX and SI are reclocked so that setup and hold times apply. The appropriate CLOCK edge must be determined from the timing diagrams.					
Rise time				5	ns
Fall time				5	ns
Clock period		80			ns
V_{IL}		ground	0	0.8	V
V_{IH}		2.0	5.0	5.0	V
Setup time	Relative to CLOCK edge			10	ns
Hold time	Relative to CLOCK edge			10	ns
Video Output					
Output swing (< VREF)			2		V_{pp}
Output swing (>VREF)			-0.5		V_{pp}
Zero signal level (=VREF)	Negative video		3.25		V
Non-linearity, INL	2% to 98% FS			1	%
Read noise	Default gain, no power supply feedthrough		800 (high gain) 200 (low gain)		µV RMS
Output load				100 // 20	kΩ // pF
Settling time	to 10 bits		55		ns
Dynamic Performance					
Integration time		2.88			µs
Clock frequency				12.5	MHz
Line rate	See Table 1				

Table 10. Specifications.

Array	Power Mode	Outputs	Power (mW)
SU256LSC	Low	1	135
		2	193
		4	310
	High	1	177
		2	236
		4	353
SU512LSC	Low	1	196
		2	255
		4	372
	High	1	276
		2	335
		4	452
SU512LC	Low	2	270
		4	386
		8	620
	High	2	354
		4	472
		8	706
SU1024LC	Low	2	392
		4	510
		8	744
	High	2	552
		4	670
		8	904

Table 11. Estimated analog power consumption for various window readout modes.

Parameter	Value	
	Min	Max
Positive Analog Supply (AVDD)	AVSS-0.3 V	AVSS+6.0 V
Positive Digital Supply (DVDD)	DVSS-0.3 V	DVSS+6.0 V
Digital Inputs	DVSS-0.3 V	DVDD+0.3 V
Pixel Input Currents		10 mA
Operating Temperature (package)	-20°C, non-LT version -115°C, LT version	80°C
Storage Temperature	-20°C	85°C
Beyond the above limits the device may be permanently damaged. Device specifications are only guaranteed when operated within rated conditions.		

Table 12. Absolute maximums.

8 Array-Specific Specifications

The following specifications are for an array temperature of 20°C with nominal operating conditions, 10 pF feedback capacitance, and autozero disabled.

8.1 Inoperable Pixel Definition

- Any pixel whose dark current is greater than the specification is considered inoperable.
- Any pixel whose optical response is outside the specification limits is considered inoperable.
- The minimum number of operable pixels between any two inoperable pixels is 5.
- The following number of inoperable pixels are allowed:

Array Length	1.45 µm Cutoff Wavelength at 20 °C	1.7 µm Cutoff Wavelength at 20 °C	2.2 µm Cutoff Wavelength at 20 °C	2.6 µm Cutoff Wavelength at -20 °C
SU256LSC	0	0	5	10
SU512LC	0	0	10	N/A
SU512LSC	5	5	10	N/A
SU1024LC	10	10	20	N/A

Table 13. Allowable Inoperable Pixels.

8.2 Dark Current

The photodiodes are nominally held at zero-bias, to within the input offset voltage (see Section 2). Any given pixel will have a dark current equal to the input offset voltage of that pixel divided by the shunt resistance. Because the input offset voltage may be positive or negative, the dark current may also have either sign. The following table lists the maximum dark current magnitude for each operable pixel with autozero disabled and is applicable to either 25 or 50 µm pixel pitches. The specifications are provided as both a dark current and a dark voltage rate (DVR). The DVR is based on the transimpedance gain of 16 nV/electron in high dynamic range mode (DVR = I_{dk} / 10.0 pF integration capacitor and gain = 2 V/Full Well Capacity in e-).

Pixel Aperture (µm)	1.45 µm Cutoff Wavelength at 20 °C		1.7 µm Cutoff Wavelength at 20 °C		2.2 µm Cutoff Wavelength at 20 °C		2.6 µm Cutoff Wavelength at -20 °C	
	Dark Current	Dark Voltage Rate (FCAP = 10 pF)	Dark Current	Dark Voltage Rate (FCAP = 10 pF)	Dark Current	Dark Voltage Rate (FCAP = 10 pF)	Dark Current	Dark Voltage Rate (FCAP = 10 pF)
25	N/A	N/A	2.2 pA	0.22 V/s	N/A	N/A	N/A	N/A
50	N/A	N/A	1.1 pA	0.11 V/s	2.75 nA	275 V/s	N/A	N/A
250	N/A	N/A	N/A	N/A	10.0 nA	1000 V/s	2.0 nA	200 V/s
500 µm & FCAP=10 pF	0.56 pA	0.056 V/s	2.8 pA	0.28 V/s	N/A	N/A	N/A	N/A
500 µm & *FCAP=0.13 pF	43 pA	* 4.3 V/s						

Table 14. Maximum dark current specifications with autozero disabled.

8.3 Optical Responsivity

The following table specifies the optical response of operable pixels:

Parameter	1.45 µm Cutoff Wavelength at 20 °C	1.7 µm Cutoff Wavelength at 20 °C	2.2 µm Cutoff Wavelength at 20 °C	2.6 µm Cutoff Wavelength at -20 °C
Peak wavelength (λ_{pk}), nominal	1.02 µm	1.5 µm	2.0 µm	2.0 µm
Quantum efficiency @ λ_{test}, min.	75%@ 1.31 µm	70% @ 1.55 µm	60% @ 1.55 µm	50% @ 1.55 µm
Average response @ λ_{test}, min. (10 pF feedback capacitance)	11.3 nV/photon	10.5 nV/photon	9 nV/photon	8 nV/photon
Response non-uniformity, max.	10%	10%	10%	10%

Table 15. Optical responsivity specification.

9 Quantum Efficiency

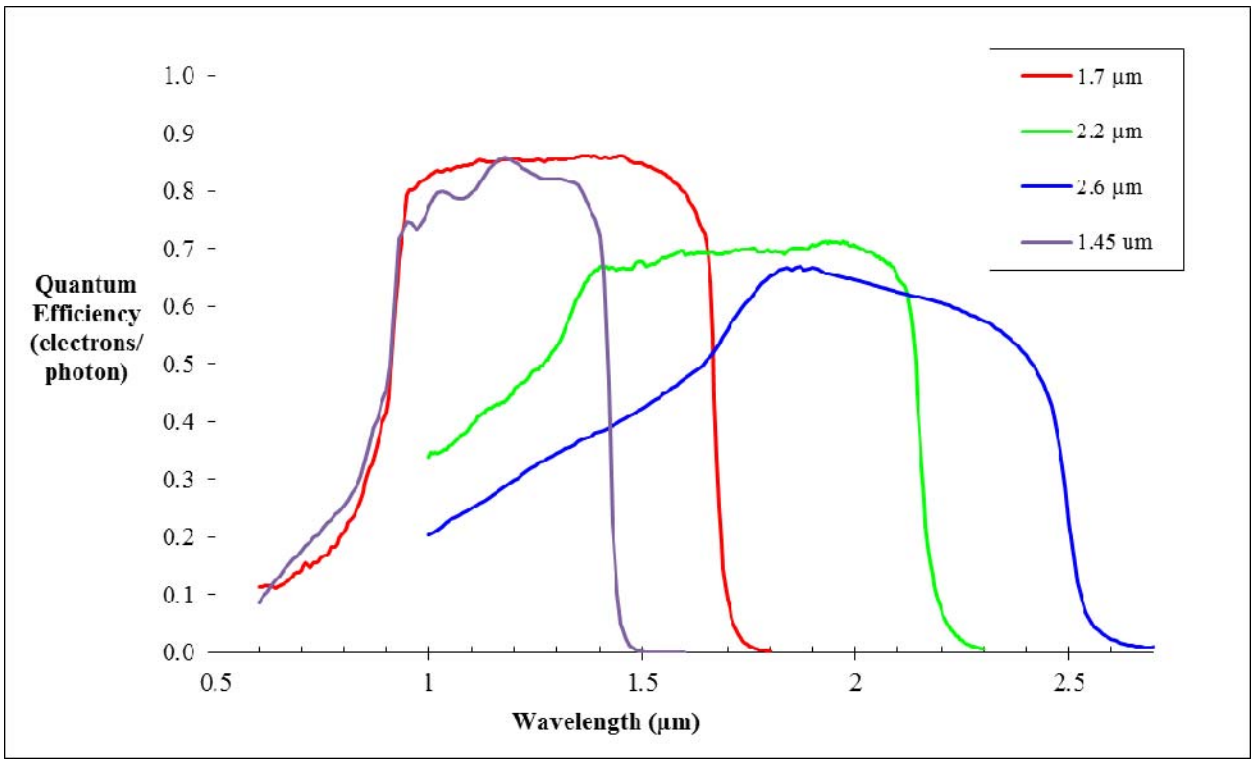


Figure 12. Representative quantum efficiency spectrum for 1.45, 1.7, 2.2 and 2.6-µm cutoff wavelength material.

InGaAs has a high QE for much of the working range, making it ideal for spectroscopy and broadband measurements. The superior D* and NEP values make it the detector of choice in its core response range.

Please take note that there is usable response down through the visible wavelengths, though it is smaller than the response to wavelengths >0.9 microns. For some applications this may be useful, though the shape of the response curve is not specified and may vary between process lots. For other applications stray visible light that reaches the detector may increase the noise level or be incorrectly read in a spectrometer as a longer wavelength signal. Optical filtering or other instrument design measures may be needed to minimize these effects.

10 Temperature Sensor

10.1 Thermistor

The thermistor is used with all versions of the array except for the LT version.

Temperature (°C)	Resistance (Ω)
-60	705,788
-55	484,294
-50	336,791
-45	237,215
-40	169,117
-35	121,968
-30	88,937
-25	65,536
-20	48,633
-15	36,539
-10	27,704
-5	21,190
0	16,344
5	12,707
10	9,956
15	7,859
20	6,247
25	5,000
30	4,027
35	3,264
40	2,662
45	2,183
50	1,800

Table 16. Typical thermistor data.

The nominal resistance of the thermistor is 5000 Ω at 25°C.

The temperature may be calculated from the thermistor resistance with the equation

$$1/T = A + B\ln(R) + C\left(\ln(R)\right)^3$$

where T is in units of Kelvin (0°C = 273.15 K) and R is in units of ohms (Ω), using the constants

$$A = 1.2891\text{x}10^{-3}$$
$$B = 2.3561\text{x}10^{-4}$$
$$C = 9.4272\text{x}10^{-8}$$

with an accuracy of ±0.5°C in the range of 0°C to 40°C.

10.2 Diode

A silicon diode is used as a temperature sensor for the LT version. The diode is a Lake Shore Cryotronics, Inc. (www.lakeshore.com) Model DT-670C-SD, which follows the curve shown below in Figure 11 (courtesy of Lake Shore Cryotronics, Inc.)

NOTE: "LT" Units shipped prior to September 2019 utilize obsoleted lakeshore model DT-471-SD. Curve available upon request.

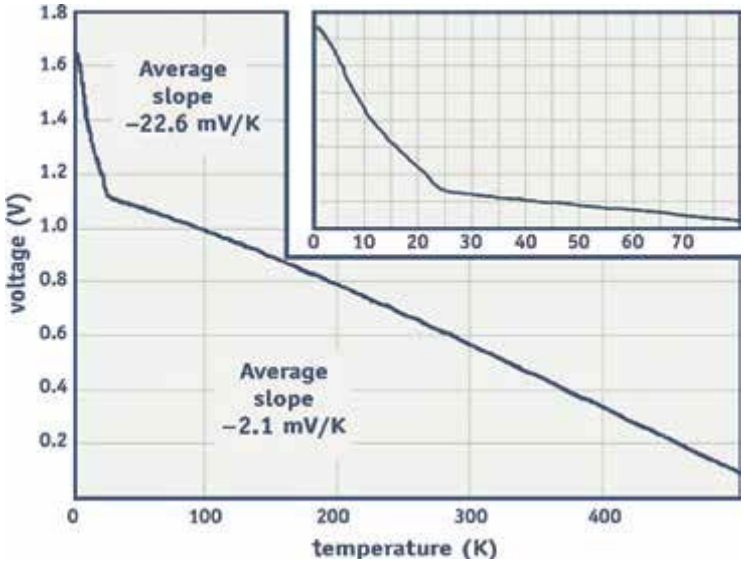


Figure 13. Voltage versus Temperature curve for silicon diode sensor used in LT version packages.

11 Thermoelectric Cooler Data

All data is for T_{hot} = 25°C and represents maximum limits for the I_{max} and V_{max} parameters. Achieving ΔT_{max} with array operating at the maximum clock rate is dependent on keeping the TEC hotside constant as the FPA is at the setpoint. Maintaining T_{hot} constant requires very good heat sink design (the mating surface to the array must be uniform and flat) and very good assembly techniques, utilizing a thin and uniform thermal compound. Thermal pads are not recommended as uneven fastening may flex the bottom of the array causing breakage of one or more thermoelectric cooler elements. See Section 13.4 for Mechanical Cautions.

Parameter	T1 (1-stage cooler)	T2 (2-stage cooler)
I_{max}	1.4 A	3.0 A
V_{max}	8.0 V	5.0 V
ΔT_{max}	> 40°C	> 50°C

Table 17. Thermoelectric cooler data.

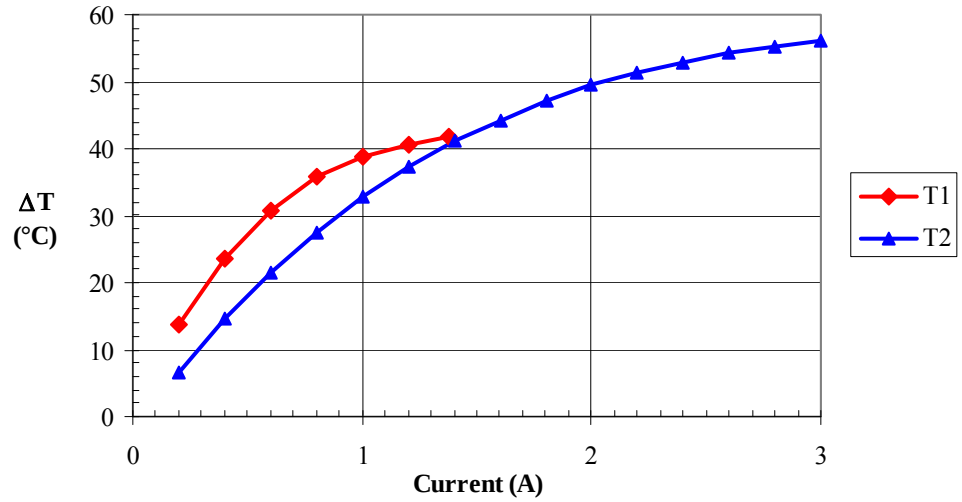


Figure 14. TEC temperature difference for the T1 and T2 versions.

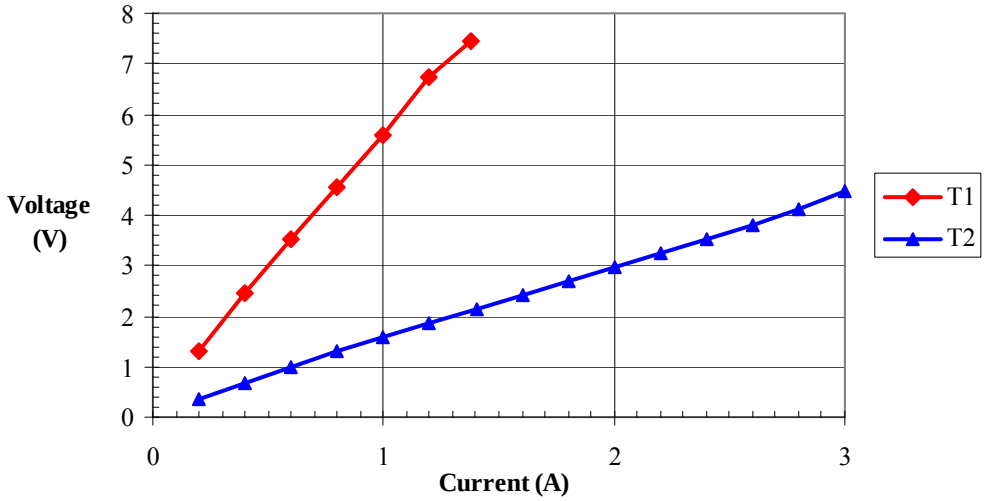


Figure 15. TEC voltage vs. current for the T1 and T2 versions.

12 Package Dimensions

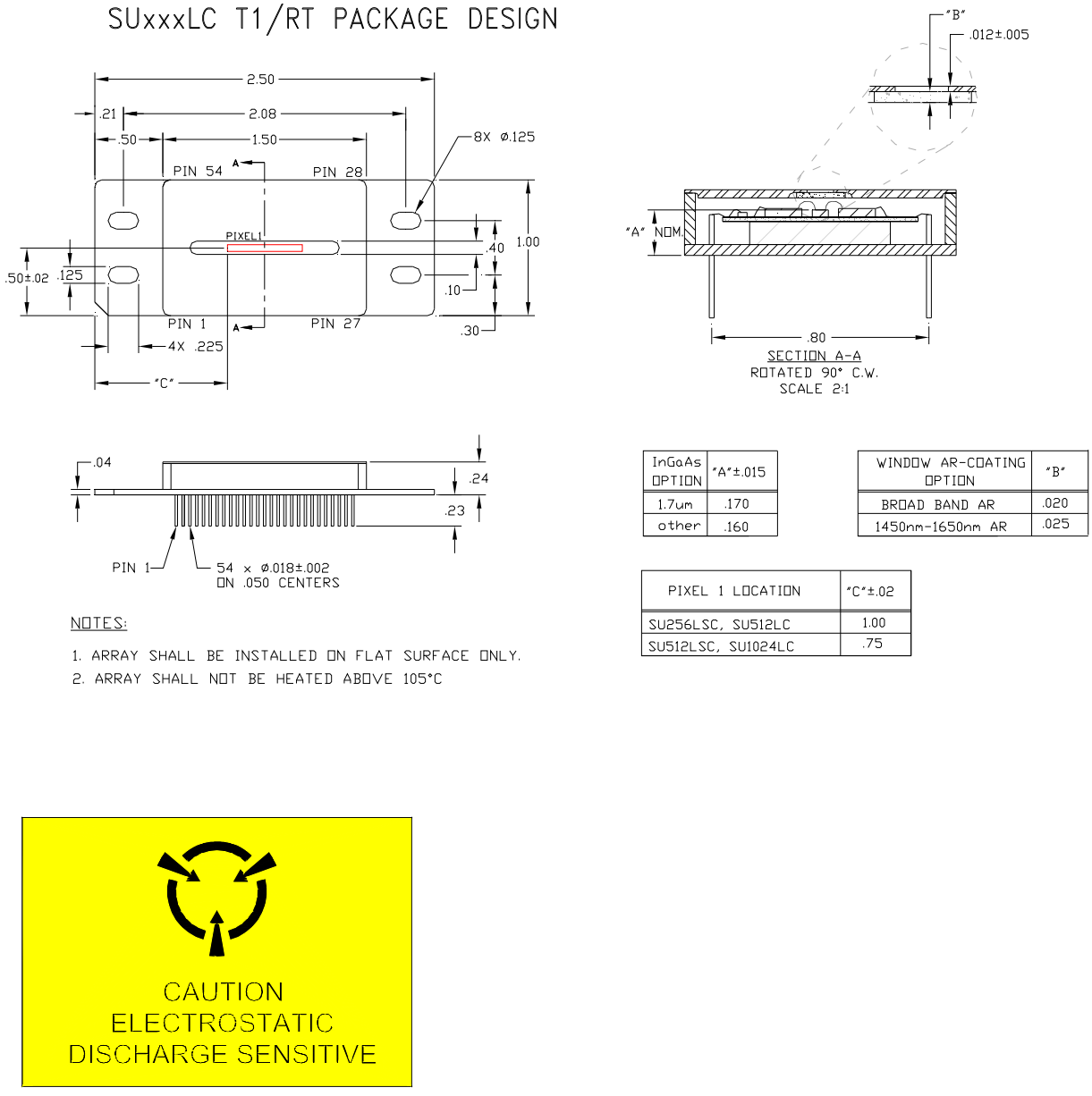
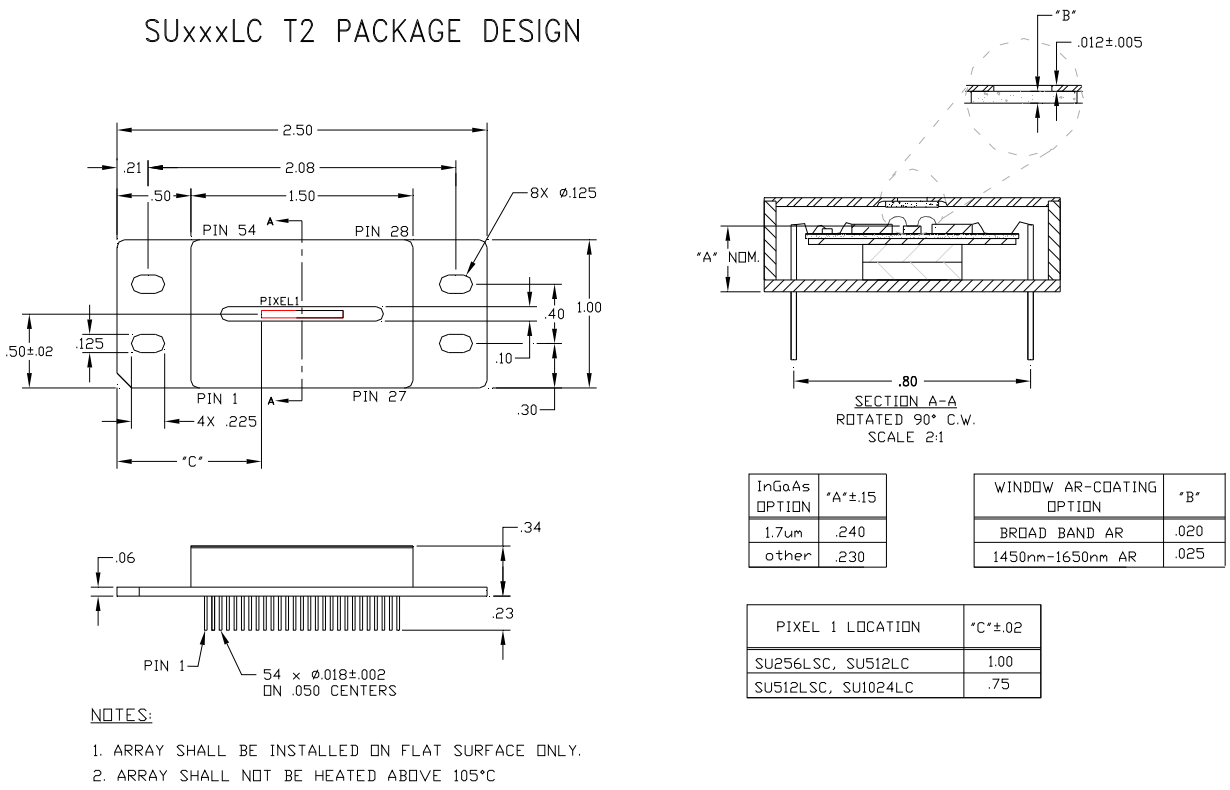


Figure 16. RT and T1 package (all dimensions are in inches).



InGaAs OPTION	"A"±.15
1.7um	.240
other	.230

WINDOW AR-COATING OPTION	"B"
BROAD BAND AR	.020
1450nm-1650nm AR	.025

PIXEL 1 LOCATION	"C"±.02
SU256LSC, SU512LC	1.00
SU512LSC, SU1024LC	.75

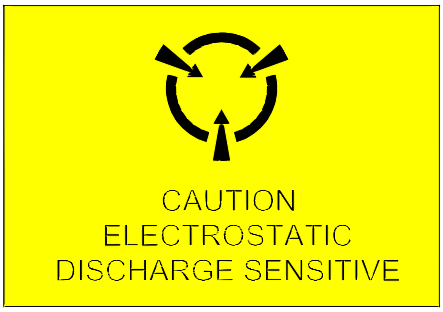


Figure 17. T2 package (all dimensions are in inches).

13 Cautions

SUI's Indium Gallium Arsenide Arrays contain both CMOS readout circuitry and, in the some versions, a thermoelectric cooler in a hermetically sealed package. When used properly, these arrays are highly reliable and rugged. The following will help the user obtain optimum performance from the device.

13.1 Electrostatic Discharge Sensitivity

Proper precautions should be taken to avoid damage from electrostatic discharge (ESD). ESD damage may range from subtle changes in performance to device failure. Please observe the following precautions:

- The device is packaged with the pins in conducting foam in an anti-static package. Open the package in a static-free environment.
- Use standard anti-static precautions such as grounded bench, floor mats and wrist straps whenever handling the device.

13.2 Thermoelectrically Cooled Versions

The thermoelectric cooler in your –T1 or –T2 model array must be used even if it is intended to operate the array at ambient temperature. The readout circuits generate heat which must be dissipated through the package. When not in use, a thermoelectric cooler is a good thermal insulator. If the cooler is not operated, the readouts will overheat and stop working and permanent damage may result.

13.3 LT Versions

The LT ("Low Temperature") version of the array uses materials to withstand low temperatures, but the cooling rate must be controlled to minimize mechanical stress. A moderate rate is 10 °C per minute.

13.4 Mechanical

When inserting the array into a socket, apply pressure only along the short edges (between pins 1 and 54 and between pins 27 and 28). This will avoid breaking the window and avoid creating internal stress that breaks the thermoelectric cooler elements. The mating surface of the heat sink for the array should be specified to have flatness within 1 mil (25.4 μm) and a roughness of less than 32 μ-inches (0.8 μm). A thin layer of thermal compound is recommended; if a thermal pad is used, ensure that the tightening the flange screws is done evenly and does not create a fulcrum that bends the base of the array.

13.5 Optical

For the 1024LC pixel square pixel array (25 μm pixel aperture), the top and bottom edges are defined by a photomask on the top surface of the front illuminated photodiodes. This creates a sharp and even imaging aperture across all of the pixels. However, for the tall pixel arrays (250 or 500 μm pixel height), and the 50 μm square pixel arrays, the top and bottom edges of the pixel are defined by the photodiode junction layout. Partially overfilling the pixels across the array may result in variation in the output intensities if all pixels are not evenly illuminated. This is especially true for the arrays with 25 μm diode pitch as there are 2 ROICs, one on each side of the photodiodes. Note that the traces to the wirebond pads can collect some signal. If one side of the array is illuminated and the other side in shadow, the pixels with connections on the illuminated side will output more signal, resulting in an odd-even variation of signal level across the array. If the optical path can be controlled to under-fill the pixel, these effects can be avoided. This effect will shift if the light image on the array shifts, which may make non-uniformity corrections difficult. Therefore, for best system non-uniformity corrections, the mechanical design of the spectrometer should limit the image height to underfill the pixel enough to allow for mechanical tolerances in the optical path. Note that this optical odd-even effect is different from the electrical odd-even variation in two output arrays. The electrical variation is the result of different gain and offset characteristics of the output amplifiers. These variations, like the variations between pixels, are stable with array temperature, and therefore are compatible with stable system non-uniformity corrections.

14 Warranty

All Sensors Unlimited products are warranted to be free from defects in workmanship and materials "Nonconformity" for a period of 12 months from the date of shipment. This warranty is limited to the repair or replacement of the unit:

> ***This warranty does not apply to products which Sensors Unlimited determines, upon inspection, have failed, become defective or unworkable due to abuse, mishandling, misuse, alteration, negligence, improper installation, use which is not in accordance with the information and precautions described in the applicable operating manual, or other causes beyond Sensors Unlimited's control.***

This warranty does not apply to (i) any products or components not manufactured by Sensors Unlimited or (ii) any aspect of the products based on Buyer's specification, unless Seller has reviewed and approved such specification in writing.

In-warranty repaired or replacement products are warranted only for the remaining non-expired portion of the original warranty period.

Except for the foregoing warranty, Sensors Unlimited specifically disclaims and excludes all other warranties, expressed or implied, including implied warranties of non-infringement, merchantability or fitness for a particular purpose.

If visible damage has occurred:

> It ***must*** be noted on all copies of the freight bill and signed by the driver. This preserves your rights and the carrier's liability.

If damage was concealed:

> Open all cartons as soon as possible! Concealed damage must be reported in writing within 5 days of receipt. Contact our shipping department for assistance between 8:00 A.M. and 5:00 P.M. EST.

All product returns require contacting the factory to request a Return Material Authorization number (RMA). End users reporting a problem should be prepared to supply the product model number, serial number, description of the problem, and relevant information about the instrumental setup, environmental conditions, user history, etc, as well as contact information. When returning a camera, all accessories, power supplies, cables and camera case should be included to ensure the user problem can be duplicated and corrected. Please visit our support web page at http://www.sensorsinc.com/customersupport.html for instructions on how to report a problem and to request return authorization.