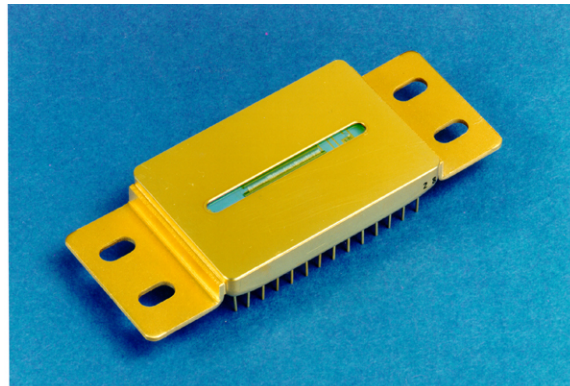


## **LDB, LSB, LE and LSE Series**

### **Linear Indium Gallium Arsenide Photodiode Arrays**



©2005-19 Sensors Unlimited, Inc., a wholly owned subsidiary of Collins Aerospace. All rights reserved.

Every effort is made to ensure the information in this manual is accurate and reliable. Use of the products described herein is understood to be at the user's risk. SUI and Collins Aerospace Corp. assumes no liability whatsoever for the use of the products detailed in this document and reserve the right to make changes in specifications at any time and without notice.

**Contents**

1	Features.....	3
2	Principles of Operation.....	3
3	Operation.....	5
3.1	General Considerations.....	5
3.2	Timing.....	5
4	Pin Assignments.....	8
5	Electrical Conditions and Performance.....	10
6	Array-Specific Specifications.....	11
6.1	Inoperable Pixel Definition.....	11
6.2	Dark Current.....	11
6.3	Optical Responsivity.....	11
7	Quantum Efficiency.....	12
8	Temperature Sensor.....	13
8.1	Thermistor.....	13
8.2	Diode.....	14
9	Thermoelectric Cooler Data.....	15
10	Package Dimensions.....	16
11	Cautions.....	19
11.1	Static Sensitivity.....	19
11.2	Thermoelectrically Cooled Versions.....	19
11.3	LT Versions.....	19
11.4	Mechanical.....	19
11.5	Optical.....	19
12	Warranty.....	20

**Tables**

Table 1.	Pin Assignments.....	8
Table 2.	Electrical Conditions.....	10
Table 3.	Electrical Performance.....	10
Table 4.	Allowable Inoperable Pixels.....	11
Table 5.	Dark current specification.....	11
Table 6.	Optical responsivity specification.....	11
Table 7.	Typical thermistor data.....	13
Table 8.	Thermoelectric cooler data.....	15

**Figures**

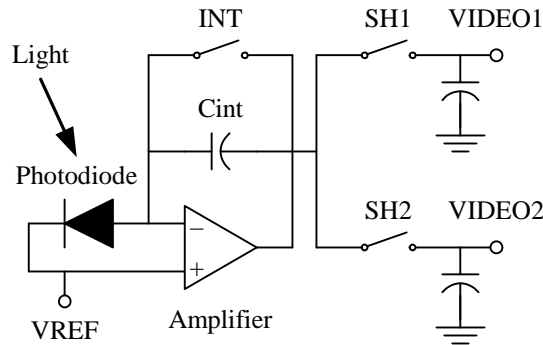
Figure 1.	Active pixel architecture. VREF, INT, SH1, and SH2 are generated internally.....	3
Figure 2.	Line sequence. LSYNC is applied, INT, SH1, and SH2 are generated internally.....	4
Figure 3.	Recommended circuit for VREF voltage connections.....	5
Figure 4.	Readout configurations, top view.....	6
Figure 5.	Overall device timing.....	6
Figure 6.	The relationship between LSYNC and CLOCK.....	7
Figure 7.	Detailed timing considerations.....	7
Figure 8.	RT, LT, T1 & T2 pin diagram, top view.....	9
Figure 9.	T3 pin diagram, top view.....	9
Figure 10.	Representative quantum efficiency spectrum for 1.45, 1.7, 2.2 & 2.6 $\mu\text{m}$ cutoff wavelength materials.....	12
Figure 11.	Voltage versus Temperature curve for silicon diode sensor used in LT version packages.....	14
Figure 12.	TEC temperature difference for T1, T2 and T3 version.....	15
Figure 13.	TEC voltage vs. current for T1, T2 and T3 versions.....	15
Figure 14.	RT and T1 package (all dimensions are in inches).....	16
Figure 15.	T2 package (all dimensions are in inches).....	17
Figure 16.	T3 package (all dimensions are in inches).....	18

Features

- Antiblooming to prevent charge overflow from saturated pixels
- Standard wavelength range of 0.8 to 1.7  $\mu\text{m}$ , a shorter range of 0.8 to 1.45  $\mu\text{m}$  or extended wavelength range of 1.1 to 2.2  $\mu\text{m}$
- SU1024LE: 1024 pixels on a 25  $\mu\text{m}$  pitch
- SU512LSE: 512 pixels on a 50  $\mu\text{m}$  pitch
- SU512LDB: 512 pixels on a 25  $\mu\text{m}$  pitch
- SU256LSB: 256 pixels on a 50  $\mu\text{m}$  pitch
- Zero inoperable pixels for standard-range devices with length less than 13 mm (1/2”), less than 1% inoperable for longer devices, and less than 2% for extended-wavelength devices
- Available with 1 or 2 stage thermoelectric cooler, or without a cooler for uncooled or externally-cooled operation.

## 1 Principles of Operation

This linear focal plane array is a hybrid combination of an InGaAs photodiode array and one or two silicon CMOS readouts. The CMOS readouts are "active pixel" devices in which the photocurrent is buffered, amplified and stored. The architecture is illustrated in Figure 1.



**Figure 1. Active pixel architecture. VREF, INT, SH1, and SH2 are generated internally.**

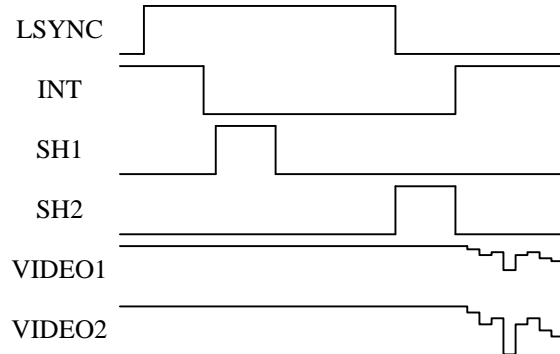
Within each readout pixel is a capacitive transimpedance amplifier (CTIA) with the photodiode at the input and the photocurrent integrated on the feedback capacitor. Two values of the feedback capacitor can be selected externally (10.4 pF and 0.4 pF). With CTIA readouts, a larger capacitor provides greater charge storage capacity and dynamic range at the expense of lower sensitivity. The choice of the two capacitors should therefore be interpreted as a choice between high dynamic range and high sensitivity modes.

Ideally, the photodiodes would be operated with zero bias to minimize dark current. Referring to Figure 1, the level of this zero bias is set by VREF and this also defines the zero signal output level. In this series of arrays, VREF is set to 3.25 V by a built-in bandgap reference voltage regulator. Due to nonuniformities in the readout, however, the actual bias across the diodes can vary over  $\pm 3$  mV. Each pixel, therefore, will exhibit a dark current of  $\Delta I = \Delta V/R_o$ ; the input offset voltage of that pixel divided by that pixel's shunt resistance. As  $\Delta V$  can vary between positive and negative levels,  $\Delta I$  can be positive or negative. This is fixed for each pixel and the dark current due to this offset appears as a fixed pattern response which extends both positively and negatively from VREF. Light induced photocurrent ('signal') will drive the output negatively from VREF. Linear operation of the pixel is specified when the output signal is limited to be within the range of 2 V negative and 1/2 V positive relative to VREF. This means that subsequent circuits should be designed to accept a range of 1.25 V to 3.75 V, with 1.25 V representing saturation by the combination of light induced photocurrent and dark current and the 3.75 V level representing saturation by positive going dark current. For valid averaging, ADC circuits should be designed to capture the full 2.5 V range and exposure times limited to avoid either saturation limit.

There are two sample-and-hold circuits at the output of the each pixel's CTIA. This allows the array to operate in a parallel-in, serial-out "snapshot" mode. Between exposures, all of the pixels are held in reset then released so that the "zero" levels can be captured with the first sample-and-holds. Following the exposure time, the "signal" levels are captured with the second sample-and-hold. The pixels are then read out sequentially. Both the initial signal

(VIDEO1) and the final signal (VIDEO2) will deviate from VREF with bipolar dark current and negative-going photocurrent.

In a typical application, VIDEO1 and VIDEO2 should be differentially amplified as a form of correlated double sampling. This eliminates much of the integrator reset switching noise. The general line sequence is shown in Figure 2. Note that the differential output will ‘foldover’ if the VIDEO2 signal saturates and the light intensity continues to increase, causing the VIDEO1 signal to also increase.



**Figure 2. Line sequence. LSYNC is applied, INT, SH1, and SH2 are generated internally.**

While waiting for a line sequence to be initiated, the CTIA feedback capacitors are held in reset. Upon initiation (the rising edge of LSYNC), the following events occur automatically:

- The INT switch is opened, which allows charge to accumulate.
- SH1 is activated to sample the signal at the start of charge integration and samples for 3 clock cycles. Signal light, dark current and the reset charge on the capacitor are captured during this sample.
- Charge continues to integrate on the feedback capacitor.

When the line sequence is terminated (on the falling edge of LSYNC), the following events occur automatically:

- SH2 is activated to sample the signal at the end of charge integration.
- The INT switch is closed, draining charge from the feedback capacitors.
- The shift registers begin operation so that the pixel-by-pixel before and after signals appear at VIDEO1 and VIDEO2 sequentially.

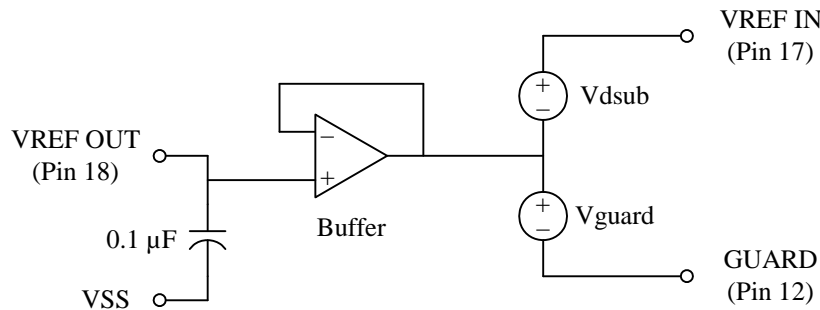
All of the above functions are generated internally. The user need only provide a continuous master clock (CLOCK) and a line-trigger pulse (LSYNC). To implement correlated double sampling, the Video 1 and 2 signals should be buffered with low-noise, low-offset buffers and those outputs connected to the inputs of a low-noise differential operational amplifier.

Devices from the LDB/LE family with photodiodes at 25 micron pitch have a separate pair of Video 1 and 2 outputs for the odd and the even pixels. When viewing the package from the top with pin 1 oriented to the top left, the right side output reads the odd pixels and the left side outputs read the even pixels. As the odd and even pixels are readout through separate circuits, the gain and offsets of those circuits will not be the same. This will usually result in an odd-even pattern in the readout signal, in addition to the fixed pattern of the photodiode and CTIA variations. For stable environmental conditions and exposure times, both fixed patterns will be quite stable. The offset variations may be minimized with simple background subtraction of an averaged set of dark scans. The amplifier gain and photodiode non-uniformity of response variations, along with the dark fixed pattern, may be removed by implementing a simple two point correction using a linear fit between the dark response and an uniform illumination at a set level of illumination such as at 50% of full scale. The device response for each pixel is linear, so stored corrections, based on averaged data to remove temporal noise, is quite effective. Single-output arrays, such as the LSB and LSE devices, only have one set of amplification circuitry and therefore do not exhibit an electrical odd-even variation. (See section 11.5 for a discussion of optical odd-even variation.)

## 2 Operation

### 2.1 General Considerations

1. The device is a mixed analog/digital integrated circuit. For power, it requires a 5 V supply.
2. It is acceptable to operate the device using a common ground (AVSS and DVSS). It is recommended that the digital signals (CLOCK and LSYNC) be operated from a separate 5 V supply (DVDD).
3. Timing is derived from a continuous master clock (CLOCK). A single control line (LSYNC) serves to initiate the exposure, determine the exposure time, and initiate the serial readout.
4. The left side and right side CLOCK pins should be connected together for two output devices.
5. If programmable logic is used to generate CLOCK and LSYNC, we recommend using 200  $\Omega$  resistors in series with the clock lines mounted as close to the source as possible. This will suppress ringing in the clock edges. The rise and fall times need to remain sharp, even if slow clock rates are used.
6. To avoid transients at the start of readout, the output amplifiers are clamped to a fixed potential when the readout circuitry is inactive (“dead”). This “dead potential” (DEADPOT) is nominally 3.25 V, which is the zero signal level (see Principles of Operation).
7. The default feedback (storage) capacitance is 0.4 pF which corresponds to high sensitivity mode. If CAP is HIGH, the feedback capacitance is increased to 10.4 pF corresponding to high dynamic range mode.
8. The double correlated output is the difference between the VIDEO1 and VIDEO2 signals. The difference may be performed in the analog domain, or VIDEO1 and VIDEO2 may be individually digitized and the difference performed in the digital domain. Either way, the load should not exceed the maximum value in Table 2.
9. A unity gain buffer should be connected with input from VREF OUT, as shown in Figure 3. VREF OUT is the reference voltage for the transimpedance amplifier, VREF IN is the connection to the photodiode substrate, and GUARD is the connection to the photodiode array guard. The buffer should be low noise and have a low input-offset to maintain the near zero-bias operation of the array. For photodiodes with a 250 or 500  $\mu\text{m}$  aperture,  $V_{\text{dsub}} = 0$  and the GUARD connection is not required as there is no internal connection for arrays with those apertures. For photodiodes with a 25 or 50  $\mu\text{m}$  aperture,  $V_{\text{guard}} = 200 \text{ mV} \pm 20 \text{ mV}$ , and  $V_{\text{dsub}}$  must be set in the range of 0 to 25 mV (with a resolution of < 1 mV) for each array to keep the array average dark output nominally zero. This may need to be adjusted if the operating temperature is changed. The total photocurrent of the array flows through VREF IN, and GUARD may draw up to 10 mA.



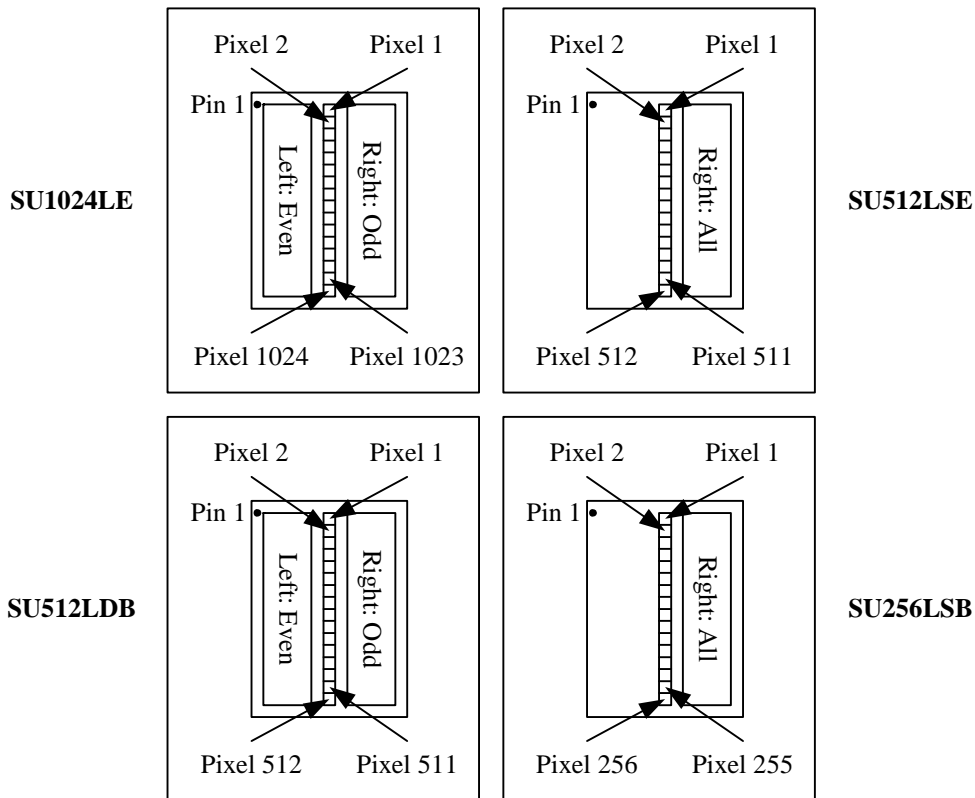
**Figure 3. Recommended circuit for VREF voltage connections.**

### 2.2 Timing

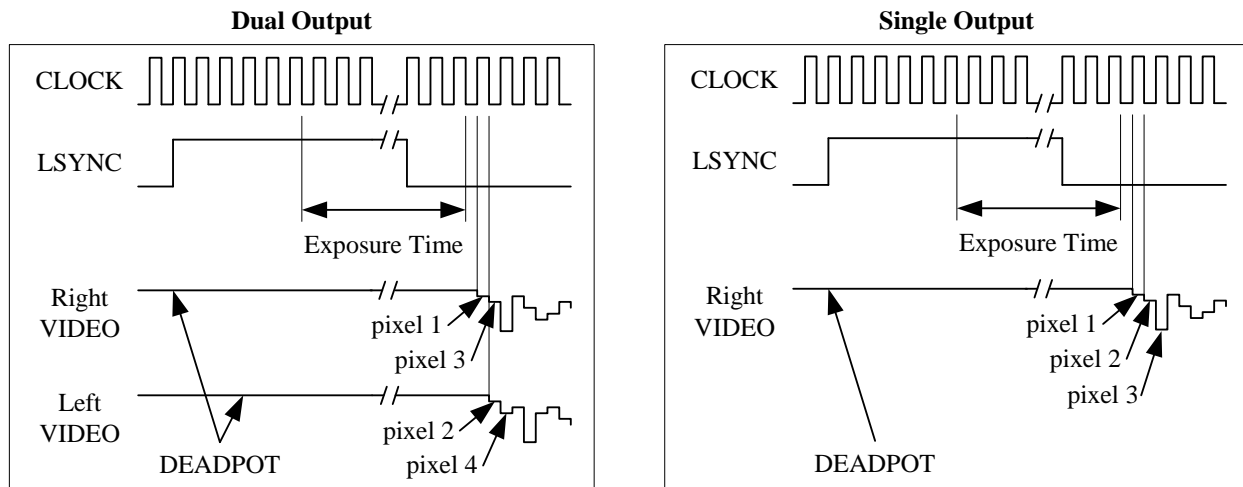
The only control signals required to operate the array are a continuous master clock (CLOCK) and an exposure time signal (LSYNC). Referring to Figure 5:

1. CLOCK should run continuously to allow internal timing functions to occur. If the clock has not run for an extended duration, or power has been recently applied, the device should be run through a complete readout cycle before the first useful exposure.
2. The CLOCK frequency should not exceed the maximum value in Table 2. Pixels are read out at both rising and falling edges of CLOCK. The maximum readout rate for each output (in units of pixels per second) is thus twice the CLOCK frequency (in Hz).

3. LSYNC should rise and fall at the rising edge of CLOCK. The minimum duration of LSYNC high is given in Table 2. The exposure time for the difference between VIDEO1 and VIDEO2 is three clock cycles less than the duration of LSYNC high.



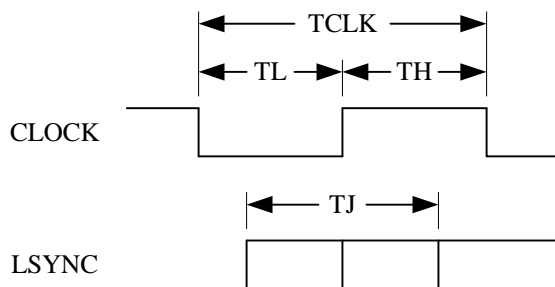
**Figure 4. Readout configurations, top view.**



**Figure 5. Overall device timing.**

4. The first pixel to emerge during readout is pixel no. 1 which is located nearest to pin 28.
5. See Figure 4 for the readout configuration. For the two-output devices, odd pixels are connected to the readouts on the right side (pins 15 and 16), and even pixels are connected to the readouts on the left side (pins 13 and 14). For the single-output devices, all pixels are connected to the readout on the right side.

6. Valid right side video will appear at VIDEO1 and VIDEO2 beginning at the 3<sup>rd</sup> rising edge of CLOCK after the falling edge of LSYNC. The left side video will appear at VIDEO1 and VIDEO2 beginning at the 4<sup>th</sup> falling edge of CLOCK. Pixels are read out at both the rising and falling edges of CLOCK.
7. The next exposure can begin anytime after the readout of the previous exposure is complete. The minimum duration of LSYNC low between exposures is given in Table 2.
8. VIDEO1 and VIDEO2 are clamped to DEADPOT in between readouts.



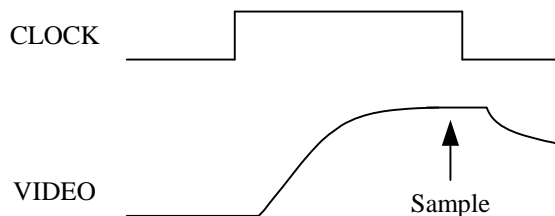
**Figure 6. The relationship between LSYNC and CLOCK.**

The detailed relationship between CLOCK and LSYNC is shown in **Error! Reference source not found.**

1. TCLK is the master clock period.
2. While it is desirable that CLOCK have a 50% duty cycle, all that is required is that both TH (the high half period) and TL (the low half period) be a minimum of 45% of TCLK.
3. Both the rising and falling edges of LSYNC should occur at the rising edge of CLOCK. The allowable jitter (TJ) is  $\pm\text{TCLK}/3$ .

The timing of the video outputs is summarized in Figure 7:

1. Video output occurs on both edges of CLOCK.
2. The sampling for analog to digital conversion should occur just before the next edge of CLOCK to maximize the settling time.



**Figure 7. Detailed timing considerations.**

### 3 Pin Assignments

The following table and figures show the pin assignments for each thermoelectric cooler option. The RT and LT versions have the same pinout as the T1, except that the RT and LT versions do not have a thermoelectric cooler (pins 3 and 26 are NC). The T3 version was an older option that is included for documentation, but is no longer offered.

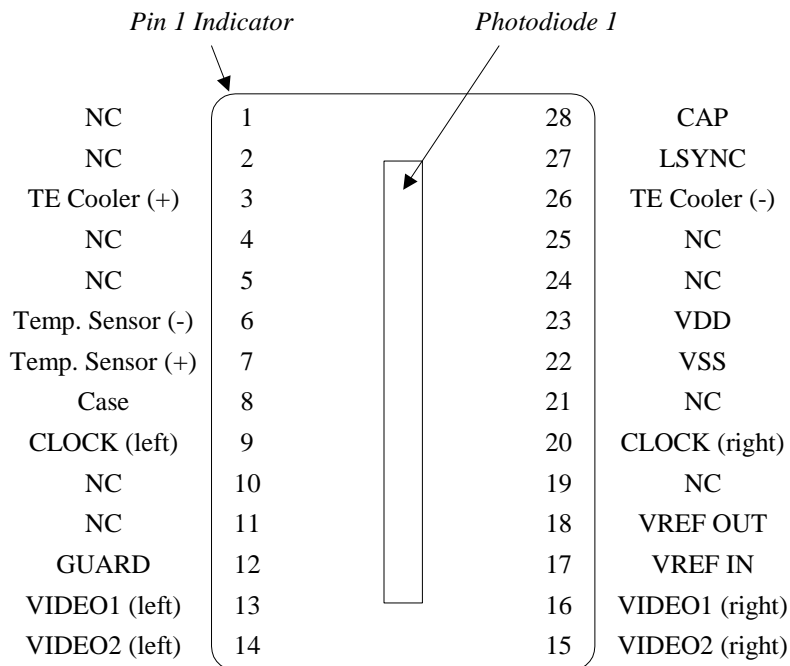
For single output devices (SU256LSB and SU512LSE shown in Figure 4), the left video connections VIDEO1 (left) and VIDEO2 (left) are not used, and it is not necessary to connect CLOCK (left).

The GUARD connection (pin 12) is only required for photodiodes with a 25 or 50  $\mu\text{m}$  aperture (height). For photodiodes with a 250 or 500  $\mu\text{m}$  aperture, the pin is internally NC but it is acceptable to apply a bias so the same board design will support either square or tall pixel arrays.

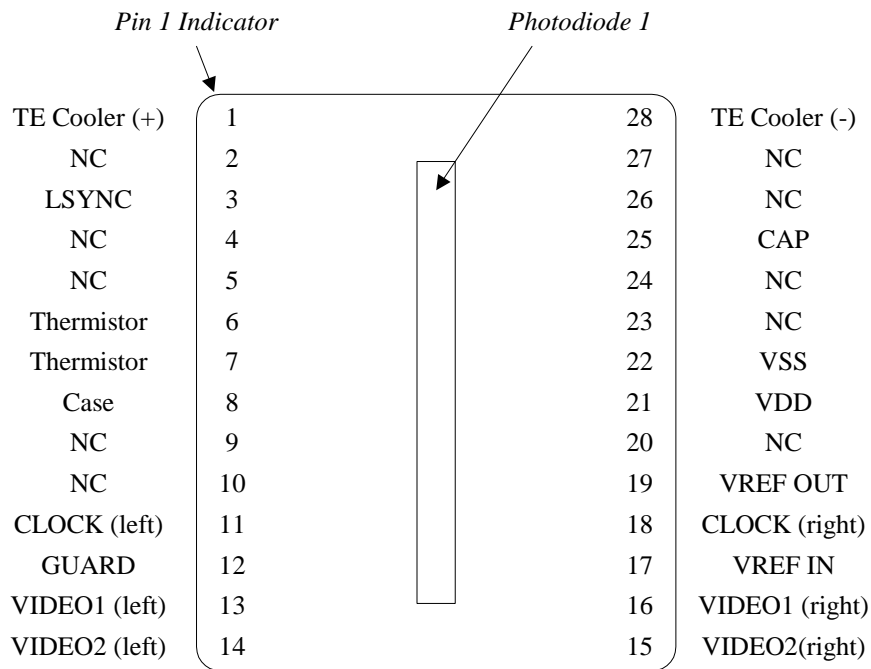
Pin	RT, LT, T1 & T2	T3
1	NC	TE Cooler (+)
2	NC	NC
3	TE Cooler (+)	LSYNC
4	NC	NC
5	NC	NC
6	Temp. Sensor (-)	Thermistor
7	Temp. Sensor (+)	Thermistor
8	Case	Case
9	CLOCK (left)	NC
10	NC	NC
11	NC	CLOCK (left)
12	GUARD	GUARD
13	VIDEO1 (left)	VIDEO1 (left)
14	VIDEO2 (left)	VIDEO2 (left)
15	VIDEO2 (right)	VIDEO2 (right)
16	VIDEO1 (right)	VIDEO1 (right)
17	VREF IN	VREF IN
18	VREF OUT	CLOCK (right)
19	NC	VREF OUT
20	CLOCK (right)	NC
21	NC	VDD
22	VSS	VSS
23	VDD	NC
24	NC	NC
25	NC	CAP
26	TE Cooler (-)	NC
27	LSYNC	NC
28	CAP	TE Cooler (-)

**Table 1. Pin Assignments.**





**Figure 8. RT, LT, T1 & T2 pin diagram, top view.**



**Figure 9. T3 pin diagram, top view.**

## 4 Electrical Conditions and Performance

Parameter	Units	Min.	Typical	Max.
V <sub>DD</sub>	V	4.90	5.00	5.25
Current (5.00 V)	mA			LE: 100 LDB: 60 LSE: 50 LSB: 30
V <sub>SS</sub>	V		0	
Case	V		0	
CLOCK HIGH	V		V <sub>DD</sub>	
LOW	V		V <sub>SS</sub>	
Frequency	Hz	1 x 10 <sup>3</sup>		1.25 x 10 <sup>6</sup>
Duty Cycle	%	45	50	55
LSYNC HIGH	V		V <sub>DD</sub>	
LOW	V		V <sub>SS</sub>	
Duration high		Longer of 6 clocks and 20 x 10 <sup>-6</sup> s		
Duration low	Clock cycles	LDB & LSB: 132, LE & LSE: 260		
CAP HIGH	V		V <sub>DD</sub>	
LOW	V		V <sub>SS</sub>	
Current (5.00 V)	μA			10
V <sub>dsub</sub> <sup>1</sup> = VREF IN - VREF OUT	V	0.000	0.010	0.025
V <sub>guard</sub> <sup>1</sup> = VREF OUT - GUARD	V	0.18	0.20	0.22
I <sub>GUARD</sub>	mA			10
Video Output Load				
Resistance	kΩ	500		
Capacitance	pF			50
Ambient Temperature				
Operating (package T)	°C	-20, non-LT version -115, LT version		80
Storage	°C	-20		85

<sup>1</sup> Values listed for square pixel arrays (25 or 50 μm aperture);  
for rectangular pixel (250 or 500 μm aperture), V<sub>dsub</sub> = 0.000 and V<sub>guard</sub> is not needed.

**Table 2. Electrical Conditions.**

Parameter	Units	Min.	Typical	Max.
DEADPOT	V		3.25	
Saturation charge (CAP = LOW)	pC		0.8	
(CAP = HIGH)	electrons		5 x 10 <sup>6</sup>	
	pC		20.8	
	electrons		130 x 10 <sup>6</sup>	
Gain (CAP = LOW)	nV/electron		400	
(CAP = HIGH)	nV/electron		15.4	
Readout noise (CAP = LOW)	electrons/√scan		800	
(CAP = HIGH)	electrons/√scan		10000	

**Table 3. Electrical Performance.**

## 5 Array-Specific Specifications

The following specifications are for an array temperature of 20°C with nominal operating conditions in the high dynamic range mode.

### 5.1 Inoperable Pixel Definition

- Any pixel whose dark current is greater than the specification is considered inoperable.
- Any pixel whose optical response is outside the specification limits is considered inoperable.
- The minimum number of operable pixels between any two inoperable pixels is 5.
- The following number of inoperable pixels are allowed:

Array Length	Allowable Inoperable Pixels	
	1.45 & 1.7 $\mu\text{m}$ Cutoff Wavelength	2.2 $\mu\text{m}$ Cutoff Wavelength
256	0	5
512 (LDB)	0	10
512 (LSE)	5	10 (15 for 500 $\mu\text{m}$ )
1024	10	20

**Table 4. Allowable Inoperable Pixels.**

### 5.2 Dark Current

The photodiodes are nominally held at zero-bias, to within the input offset voltage (see Section 2). Any given pixel will have a dark current equal to the input offset voltage of that pixel divided by the shunt resistance. Because the input offset voltage may be positive or negative, the dark current may also have either sign. The following table lists the maximum dark current magnitude for each operable pixel. The specifications are provided as both a dark current and a dark voltage rate (DVR). The DVR is based on the transimpedance gain of 15 nV/electron in high dynamic range mode ( $\text{DVR} = I_{\text{dk}} / 10.4 \text{ pF}$  integration capacitor and gain = 2 V/Full Well Capacity in e-).

Pixel Aperture ( $\mu\text{m}$ )	1.45 $\mu\text{m}$ Cutoff Wavelength			1.7 $\mu\text{m}$ Cutoff Wavelength			2.2 $\mu\text{m}$ Cutoff Wavelength		
	Dark Current	Dark Voltage Rate		Dark Current	Dark Voltage Rate		Dark Current	Dark Voltage Rate	
	Maximum	Max	Mean	Maximum	Max	Mean	Maximum	Max	Mean
25	-	-	-	2.2 pA	0.22 V/s	0.09 V/s	-	-	-
50	-	-	-	1.1 pA	0.11 V/s	0.028 V/s	2.75 nA	275 V/s	110 V/s
250	-	-	-	-	-	-	10.0 nA	1000 V/s	250 V/s
500	x.x pA	0.xx V/s	0.0xx V/s	2.8 pA	0.28 V/s	0.068 V/s	14.5 nA	1450 V/s	360 V/s

**Table 5. Dark current specification.**

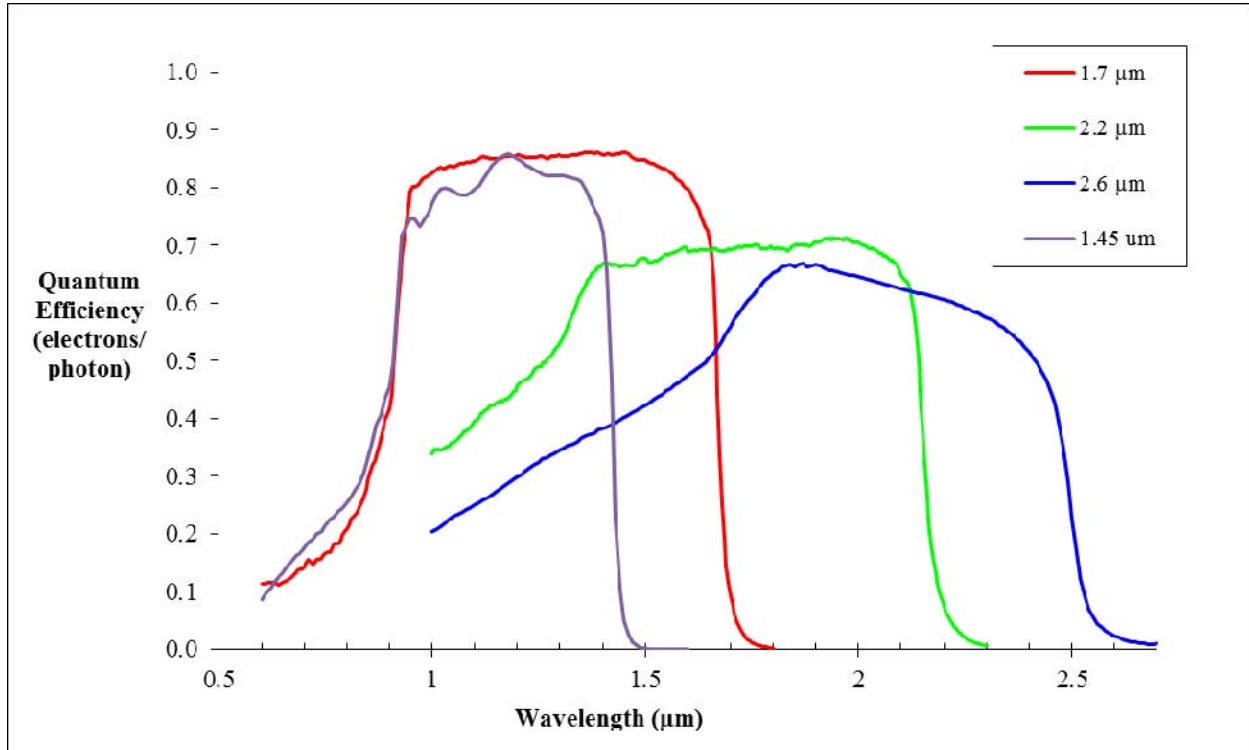
### 5.3 Optical Responsivity

The following table specifies the optical response of operable pixels:

Parameter	1.45 $\mu\text{m}$ Cutoff Wavelength	1.7 $\mu\text{m}$ Cutoff Wavelength	2.2 $\mu\text{m}$ Cutoff Wavelength
Peak wavelength ( $\lambda_{\text{pk}}$ ), nominal	1.02 $\mu\text{m}$	1.5 $\mu\text{m}$	2.0 $\mu\text{m}$
Quantum efficiency @ $\lambda_{\text{test}}$ , minimum	75% @ 1.31 $\mu\text{m}$	70% @ 1.55 $\mu\text{m}$	60% @ 1.55 $\mu\text{m}$
Average array response @ $\lambda_{\text{pk}}$ , minimum (high dynamic range mode – 10.4 pF)	11.3 nV/photon	10.5 nV/photon	9 nV/photon
Response non-uniformity, maximum	10%	10%	10%

**Table 6. Optical responsivity specification.**

## 6 Quantum Efficiency



**Figure 10. Representative quantum efficiency spectrum for 1.45, 1.7, 2.2 & 2.6 μm cutoff wavelength materials.**

InGaAs has a high QE for much of the working range, making it ideal for spectroscopy and broadband measurements. The superior  $D^*$  and NEP values make it the detector of choice in its core response range. Please take note that there is usable response down through the visible wavelengths, though it is smaller than the response to wavelengths  $>0.9$  microns. For some applications this may be useful, though the shape of the response curve is not specified and may vary between process lots. For other applications stray visible light that reaches the detector may increase the noise level or be incorrectly read in a spectrometer as a longer wavelength signal. Optical filtering or other instrument design measures may be needed to minimize these effects.

## 7 Temperature Sensor

### 7.1 Thermistor

The thermistor is used with all versions of the array except for the LT version.

Temperature (°C)	Resistance (Ω)
-60	705,788
-55	484,294
-50	336,791
-45	237,215
-40	169,117
-35	121,968
-30	88,937
-25	65,536
-20	48,633
-15	36,539
-10	27,704
-5	21,190
0	16,344
5	12,707
10	9,956
15	7,859
20	6,247
25	5,000
30	4,027
35	3,264
40	2,662
45	2,183
50	1,800

**Table 7. Typical thermistor data.**

The nominal resistance of the thermistor is 5000 Ω at 25°C.

The temperature may be calculated from the thermistor resistance with the equation

$$1/T = A + B \ln(R) + C(\ln(R))^3$$

where  $T$  is in units of Kelvin ( $0^\circ\text{C} = 273.15\text{ K}$ ) and  $R$  is in units of ohms ( $\Omega$ ), using the constants

$$A = 1.2891 \times 10^{-3}$$

$$B = 2.3561 \times 10^{-4}$$

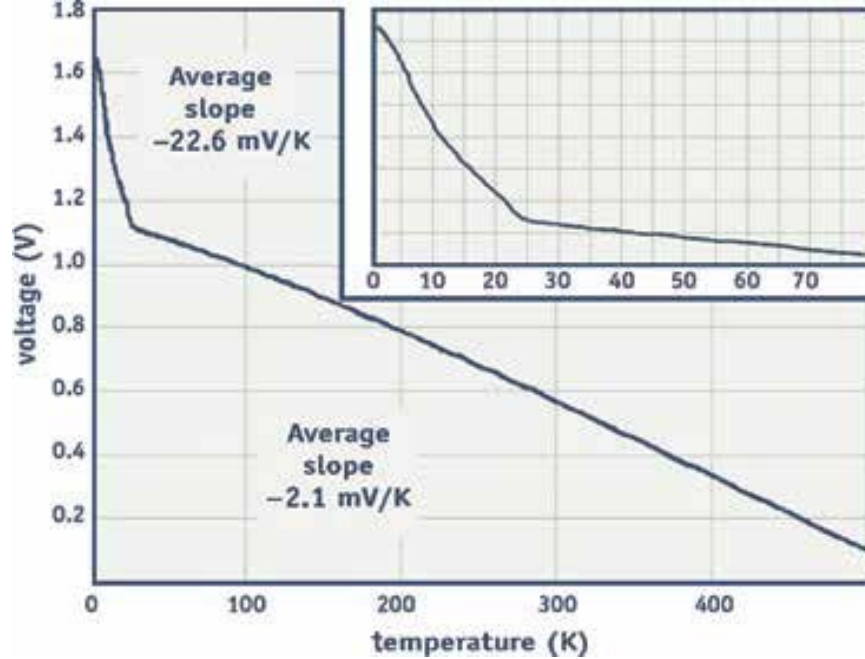
$$C = 9.4272 \times 10^{-8}$$

with an accuracy of  $\pm 0.5^\circ\text{C}$  in the range of  $0^\circ\text{C}$  to  $40^\circ\text{C}$ .

**7.2 Diode**

A silicon diode is used as a temperature sensor for the LT version. The diode is a Lake Shore Cryotronics, Inc. ([www.lakeshore.com](http://www.lakeshore.com)) Model DT-670C-SD, which follows the curve shown below in Figure 11 (courtesy of Lake Shore Cryotronics, Inc.)

**NOTE: "LT" Units shipped prior to September 2019 utilize obsoleted lakeshore model DT-471-SD. Curve available upon request.**



**Figure 11. Voltage versus Temperature curve for silicon diode sensor used in LT version packages.**

## 8 Thermoelectric Cooler Data

All data is for  $T_{hot} = 25^{\circ}\text{C}$  and represents maximum limits for the  $I_{max}$  and  $V_{max}$  parameters. Achieving  $\Delta T_{max}$  with array operating at the maximum clock rate is dependent on keeping the TEC hotside constant as the FPA is at the setpoint. Maintaining  $T_{hot}$  constant requires very good heat sink design (the mating surface to the array must be uniform and flat) and very good assembly techniques, utilizing a thin and uniform thermal compound. Thermal pads are not recommended as uneven fastening may flex the bottom of the array causing breakage of one or more thermoelectric cooler elements. (Note: The T3 version is no longer in production)

Parameter	T1 (1-stage cooler)	T2 (2-stage cooler)	T3 (3-stage cooler)
$I_{max}$	1.4 A	2.4 A	3.4 A
$V_{max}$	8.0 V	5.0 V	7.3 V
$\Delta T_{max}$	> 40°C	> 50°C	> 70°C

Table 8. Thermoelectric cooler data.

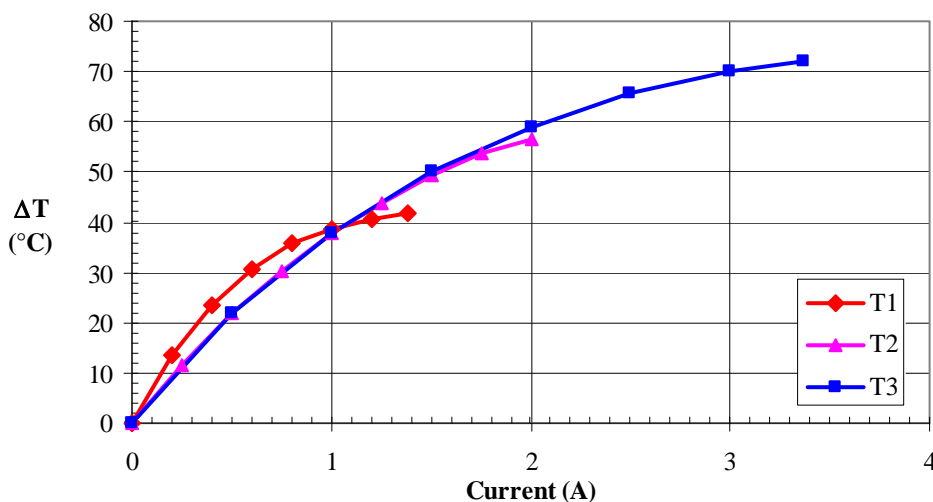


Figure 12. TEC temperature difference for T1, T2 and T3 version.

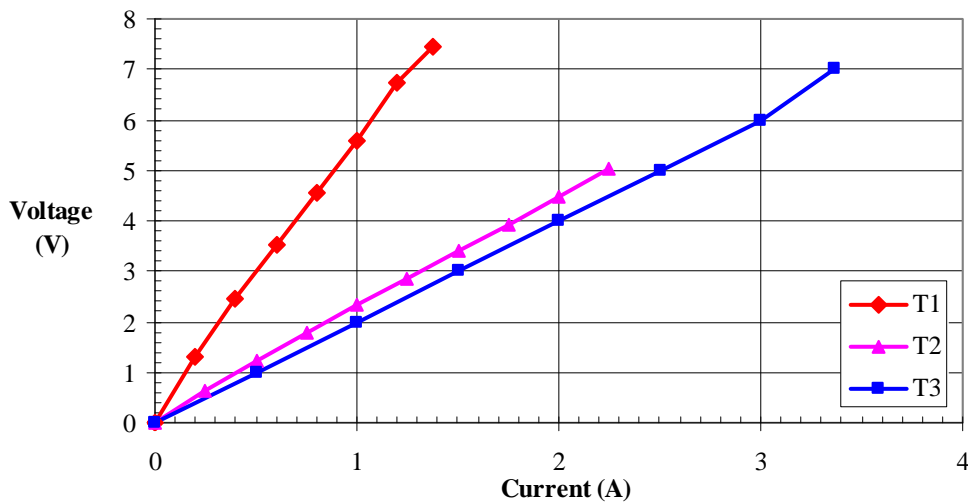
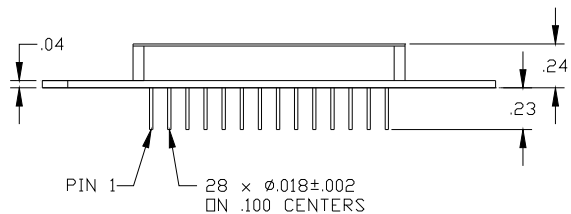
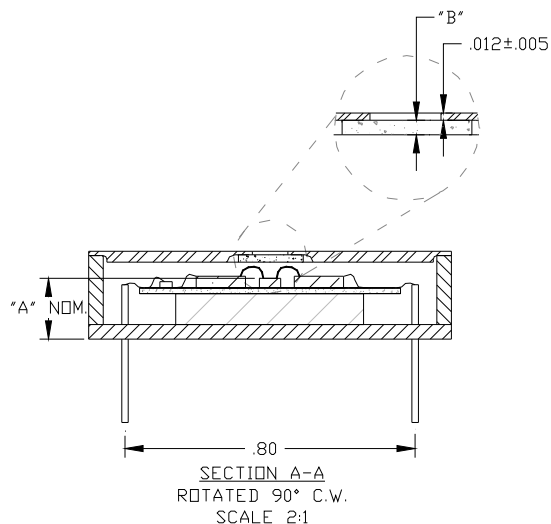
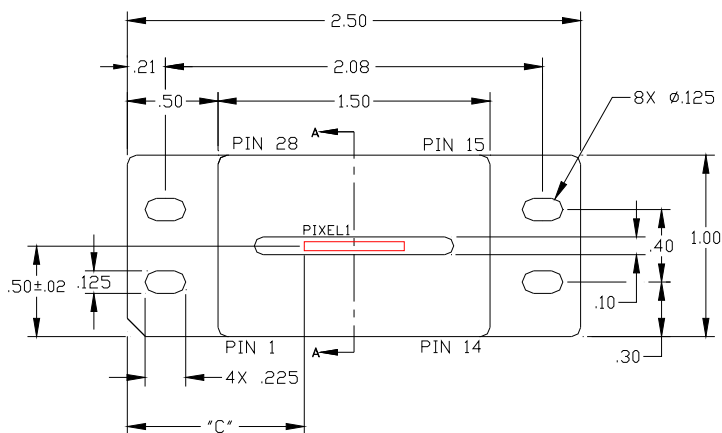


Figure 13. TEC voltage vs. current for T1, T2 and T3 versions.

## 9 Package Dimensions

### SUxxxL T1/RT PACKAGE DESIGN



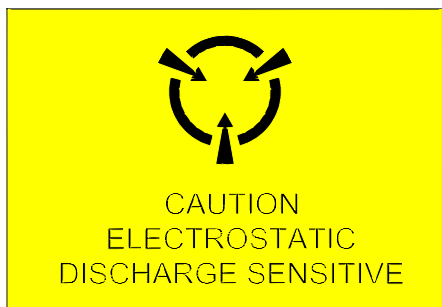
**NOTES:**

1. ARRAY SHALL BE INSTALLED ON FLAT SURFACE ONLY.
2. ARRAY SHALL NOT BE HEATED ABOVE 105°C

InGaAs OPTION	"A" ± .015
1.7um	.170
2.2um	.160

WINDOW AR-COATING OPTION	"B"
BROAD BAND AR	.020
1450nm-1650nm AR	.025

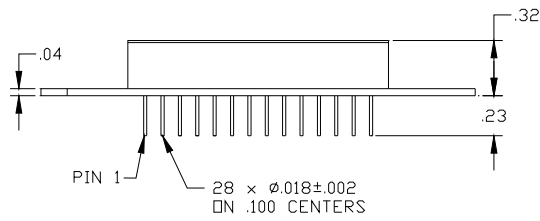
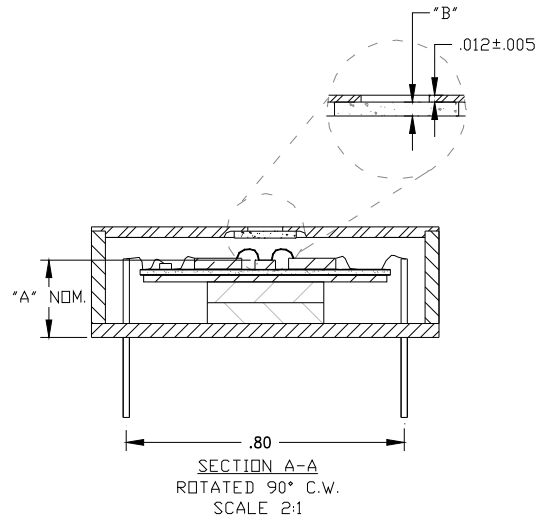
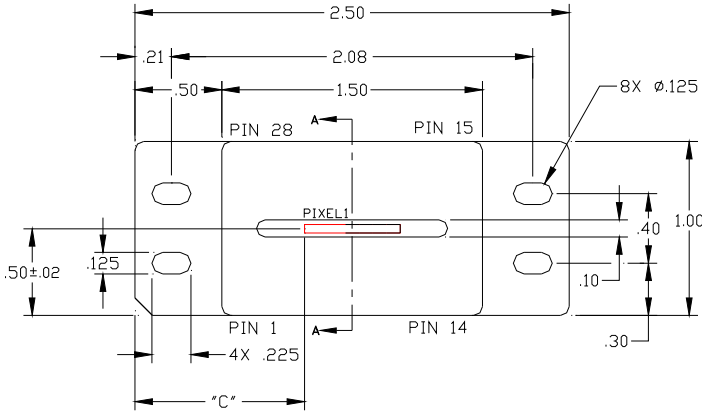
PIXEL 1 LOCATION	"C" ± .02
SUxxxLDB, SUxxxLSB	1.00
SUxxxLE, SUxxxLSE	.75



**Figure 14. RT and T1 package (all dimensions are in inches).**



**SUxxxL T2 PACKAGE DESIGN**



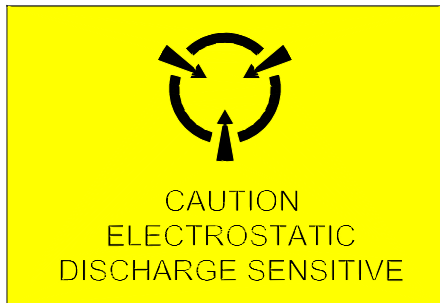
InGaAs OPTION	*A*±.15
1.7µm	.220
2.2µm	.210

WINDOW AR-COATING OPTION	*B*
BROAD BAND AR	.020
1450nm-1650nm AR	.025

PIXEL 1 LOCATION	*C*±.02
SUxxxLDB, SUxxxLSB	1.00
SUxxxLE, SUxxxLSE	.75

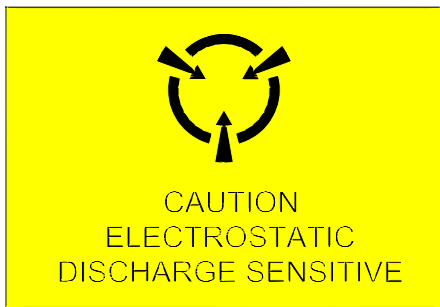
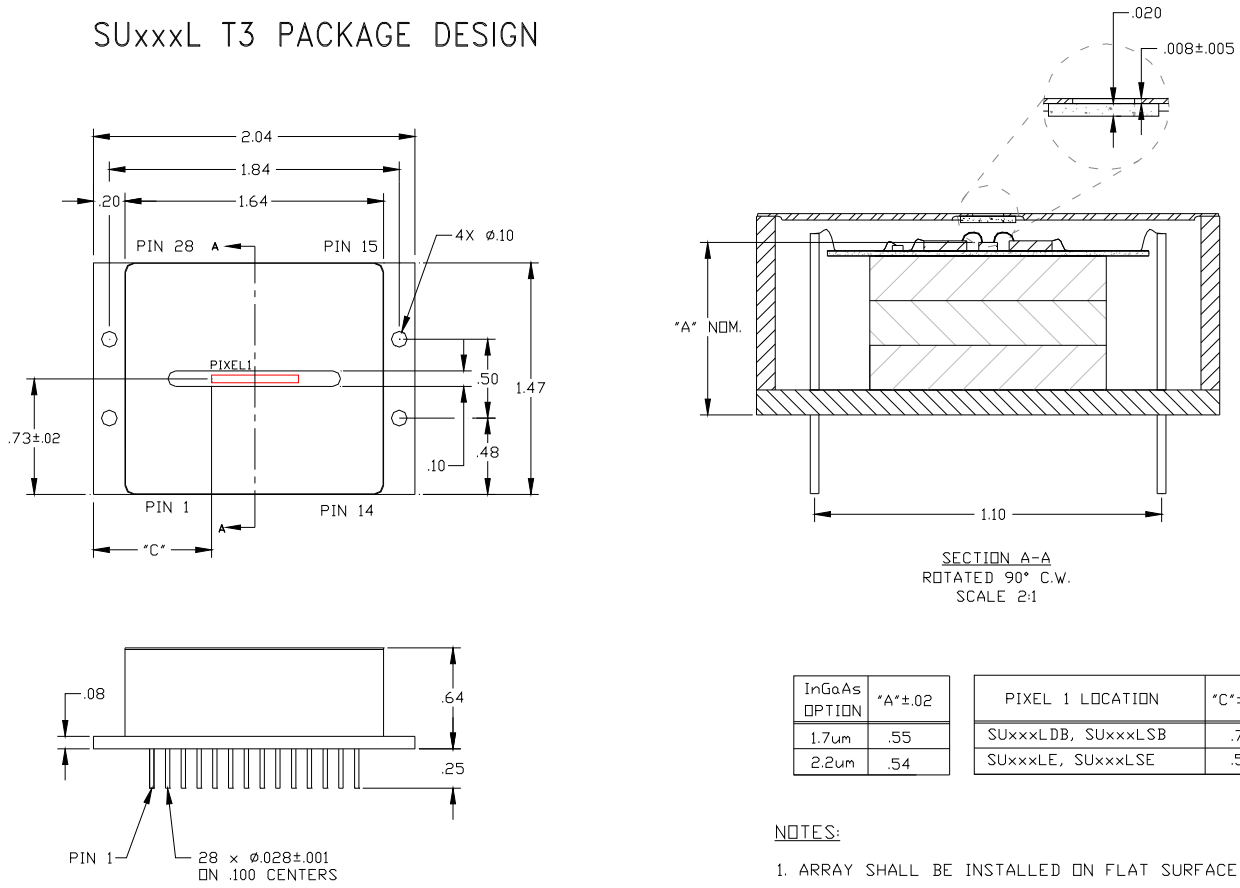
**NOTES:**

1. ARRAY SHALL BE INSTALLED ON FLAT SURFACE ONLY.
2. ARRAY SHALL NOT BE HEATED ABOVE 105°C



**Figure 15. T2 package (all dimensions are in inches).**

**SUxxxL T3 PACKAGE DESIGN**



**Figure 16. T3 package (all dimensions are in inches).**

## 10 Cautions

Sensors Unlimited's Indium Gallium Arsenide Arrays contain both CMOS readout circuitry and, in the some versions, a thermoelectric cooler in a hermetically sealed package. When used properly, these arrays are highly reliable and rugged. The following will help the user obtain optimum performance from the device.

### 10.1 Static Sensitivity

The CMOS readouts are extremely sensitive to static discharge. Please observe the following precautions:

- The device is packaged with the pins in conducting foam in an anti-static package. Open the package in a static-free environment.
- Use standard anti-static precautions such as grounded bench, floor mats and wrist straps whenever handling the device.
- Pin 8 of the device is connected to the case. In your circuitry, pin 8 should be connected to earth ground with care taken to avoid ground loops to supply or signal grounds.

### 10.2 Thermoelectrically Cooled Versions

The thermoelectric cooler in your array must be used even if it is intended to operate the array at ambient temperature. The readout circuits generate heat which must be dissipated through the package. When not in use, a thermoelectric cooler is a good thermal insulator. If the cooler is not operated, the readouts will overheat and stop working and permanent damage may result.

### 10.3 LT Versions

The LT ("Low Temperature") version of the array uses materials to withstand low temperatures, but the cooling rate must be controlled to minimize mechanical stress. A moderate rate is 10 °C per minute.

### 10.4 Mechanical

When inserting the array into a socket, apply pressure only along the short edges (between pins 1 and 28 and between pins 14 and 15). This is to avoid breaking the window and to avoid creating internal stress that breaks the thermoelectric cooler elements. The mating surface of the heat sink for the array should be specified to have flatness within 1 mil (25.4 μm) and a roughness of less than 32 μ-inches (0.8 μm). A thin layer of thermal compound is recommended; if a thermal pad is used, ensure that the tightening the flange screws is done evenly and does not create a fulcrum that bends the base of the array.

### 10.5 Optical

For the tall pixel arrays (250 or 500 μm pixel height), and the 50 μm square pixel arrays, the top and bottom edges of the pixel are defined by the photodiode junction layout. Partially overfilling the pixels across the array may result in variation in the output intensities if all pixels are not evenly illuminated. This is especially true for the arrays with 25 μm diode pitch as there are 2 ROICs, one on each side of the photodiodes. Note that the traces to the wirebond pads can collect some signal. If one side of the array is illuminated and the other side in shadow, the pixels with connections on the illuminated side will output more signal, resulting in an odd-even variation of signal level across the array. If the optical path can be controlled to under-fill the pixel, these effects can be avoided. This effect will shift if the light image on the array shifts, which may make non-uniformity corrections difficult. Therefore, for best system non-uniformity corrections, the mechanical design of the spectrometer should limit the image height to underfill the pixel enough to allow for mechanical tolerances in the optical path. Note that this optical odd-even effect is different from the electrical odd-even variation in two output arrays. The electrical variation is the result of different gain and offset characteristics of the output amplifiers. These variations, like the variations between pixels, are stable with array temperature, and therefore is compatible with stable system non-uniformity corrections.

## 11 Warranty

All Sensors Unlimited products are warranted to be free from defects in workmanship and materials “Nonconformity” for a period of 12 months from the date of shipment. This warranty is limited to the repair or replacement of the unit:

*This warranty does not apply to products which Sensors Unlimited determines, upon inspection, have failed, become defective or unworkable due to abuse, mishandling, misuse, alteration, negligence, improper installation, use which is not in accordance with the information and precautions described in the applicable operating manual, or other causes beyond Sensors Unlimited’s control.*

This warranty does not apply to (i) any products or components not manufactured by Sensors Unlimited or (ii) any aspect of the products based on Buyer’s specification, unless Seller has reviewed and approved such specification in writing.

In-warranty repaired or replacement products are warranted only for the remaining non-expired portion of the original warranty period.

Except for the foregoing warranty, Sensors Unlimited specifically disclaims and excludes all other warranties, expressed or implied, including implied warranties of non-infringement, merchantability or fitness for a particular purpose.

### **If visible damage has occurred:**

It *must* be noted on all copies of the freight bill and signed by the driver. This preserves your rights and the carrier’s liability.

### **If damage was concealed:**

Open all cartons as soon as possible! Concealed damage must be reported in writing within 5 days of receipt. Contact our shipping department for assistance between 8:00 A.M. and 5:00 P.M. EST.

All product returns require contacting the factory to request a Return Material Authorization number (RMA). End users reporting a problem should be prepared to supply the product model number, serial number, description of the problem, and relevant information about the instrumental setup, environmental conditions, user history, etc, as well as contact information. When returning a camera, all accessories, power supplies, cables and camera case should be included to ensure the user problem can be duplicated and corrected. Please visit our support web page at <http://www.sensorsinc.com/company/support-services/> for instructions on how to report a problem and to request return authorization.