TRUPACK MULTI-PROCESSOR SYSTEM IN PACKAGE (MPSIP)
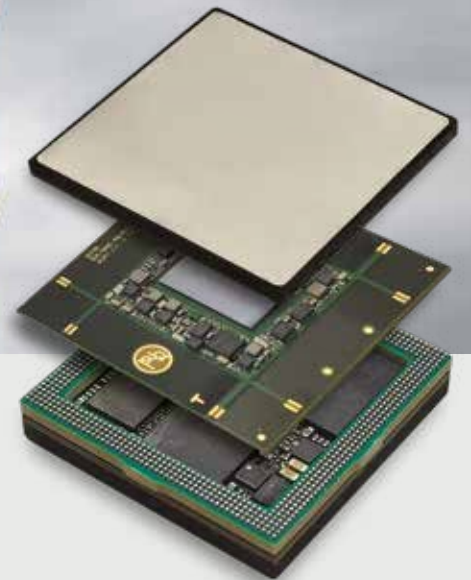
SECURE PROCESSING

Advanced capabilities with a small footprint

With the growing demand for versatile microelectronics, Collins Aerospace delivers with TruPack Multi-Processor System in Package (MPSiP) technology for secure processing in multiple applications, including edge processing, system control and sensor aggregation.

Collins TruPack SiP integrates with Xilinx Zynq™ Ultrascale+™ Multi-Processor System on Chip (MPSoC) combining power management, clock management,

RAM, program flash and the MPSoC in a low SWaP-C package. The TruPack SiP is configurable to meet the varying security needs of US Government military systems. Additionally it is manufactured in our Defense Microelectronics Activity-certified facility enhancing the supply-chain trust needed to ensure the TruPack SiP will operate free of any unintended operations.
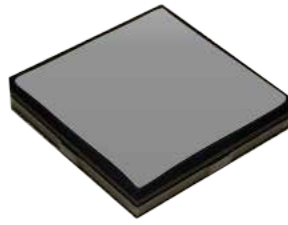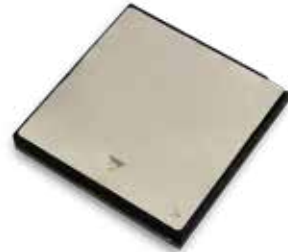
Packaged into the same footprint as the Xilinx Zynq Ultrascale+, our Trupack SIP is 20-times smaller than discrete designs. When size and security are your most important requirements, choose TruPack.

KEY FEATURES & BENEFITS

- Integrated power conversion, clock generation, memory and startup sequencing in one ball grid array (BGA)

- Faster software and host board development

- Single 5V power input

- Built-in power sequencing for the on-board SoC

- Internal reference clock and clock distribution

- Built-in LPDDR4 RAM and SoC boot flash

Collins Aerospace
An **RTX** Business

TruPack5 and TruPack11 specifications

		TRUPACK5	TRUPACK11
SoC Core		Xilinx ZU5EV	Xilinx ZU11EG
Voltage in		3.7 volts to 5.5 volts	3.7 volts to 5.5 volts
Power consumption	PS only Heavy PS + PL	3 W 20 W	7 W 35 W
Size		26 mm x 26 mm x 4.7 mm 1 in. x 1 in.x 0.18 in.	35 mm x 35 mm x 5.4 mm 1.4 in. x 1.4 in x 0.21 in.
Weight		12 g 0.42 oz	25 g 0.88 oz
Environmental	Junction temperature	- 40 ° C to 125 ° C	- 40 ° C to 100 ° C
Nonvolatile memory		2 Gb NOR Flash 4 bit Quad SPI	2 Gb NOR Flash 4 bit Quad SPI
PS RAM		4 GB LPDDR4, one 32 bit lane	4 GB LPDDR4, one 32 bit lane
Clock source		25 MHz internal reference oscillator or 5 to 710 MHz external clock	25 MHz internal reference oscillator or 5 to 710 MHz external clock
High speed Transceivers	High speed SERDES (GTY) Med speed SERDES (GTH) Low speed SERDES (GTR)	16 @ 16 Gbps 4 @ 6 Gbps	16 @ 28 Gbps 32 @ 16 Gbps 4 @ 6 Gbps
MPSoC general purpose I/O	HDIO HPIO PSMIO µcontroller I/O pins	92 64 (12 differential pairs) 70 20	79 74 (34 differential pairs) 63 23
Enhanced security		Available	Available
Export category		ITAR XI(c)(2)	ECCN 0A614.x
HTS		8542.31.00.01	8542.31.00.01

Specifications subject to change without notice.